Intel® DBPXA250 Development Platform for Intel® Personal Internet Client Architecture

User's Guide

September 2002

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Note: This revision of the *Intel® DBPXA250 Development Platform for Intel® Personal Internet Client Architecture User's Guide* pertains to Revisions E and F of the Intel® DCPXA250 processor card (the DCPXA250 processor card.)

The Intel® XScale™ microarchitecture is designed for high performance and low power. The Intel® DBPXA250 development platform (the DBPXA250 platform) provides a development system for the following Intel® application-specific processors. These processors are intended for applications requiring high performance, low power, and a high degree of integration, such as personal digital assistants, communicators, smartphones, and wireless PC companions.

- The Intel® PXA250 applications processor (the PXA250 processor) features a 32-bit data bus, operation up to 400 MHz, and a 17 x 17 mm mBGA package. The DCPXA250 processor card is supplied as standard equipment with the DBPXA250 platform kit.
- The Intel® PXA210 applications processor features a 16-bit data bus, operation up to 200 MHz, and a 13 x 13 mm TPBGA package. Contact Intel to order the Intel® DCPXA210 processor card.

The DCPXA250 or DCPXA210 processor card plugs into the Intel® BBPXA2xx development baseboard (the BBPXA2xx baseboard) to complete the DBPXA250 platform.

This chapter contains:

Chapter 2, "Hardware Description" and Chapter 3, "Programming Guide" provide detailed instructions for using the DBPXA250 platform.

1.1 Features

The DBPXA250 platform offers many features to facilitate the development of applications:

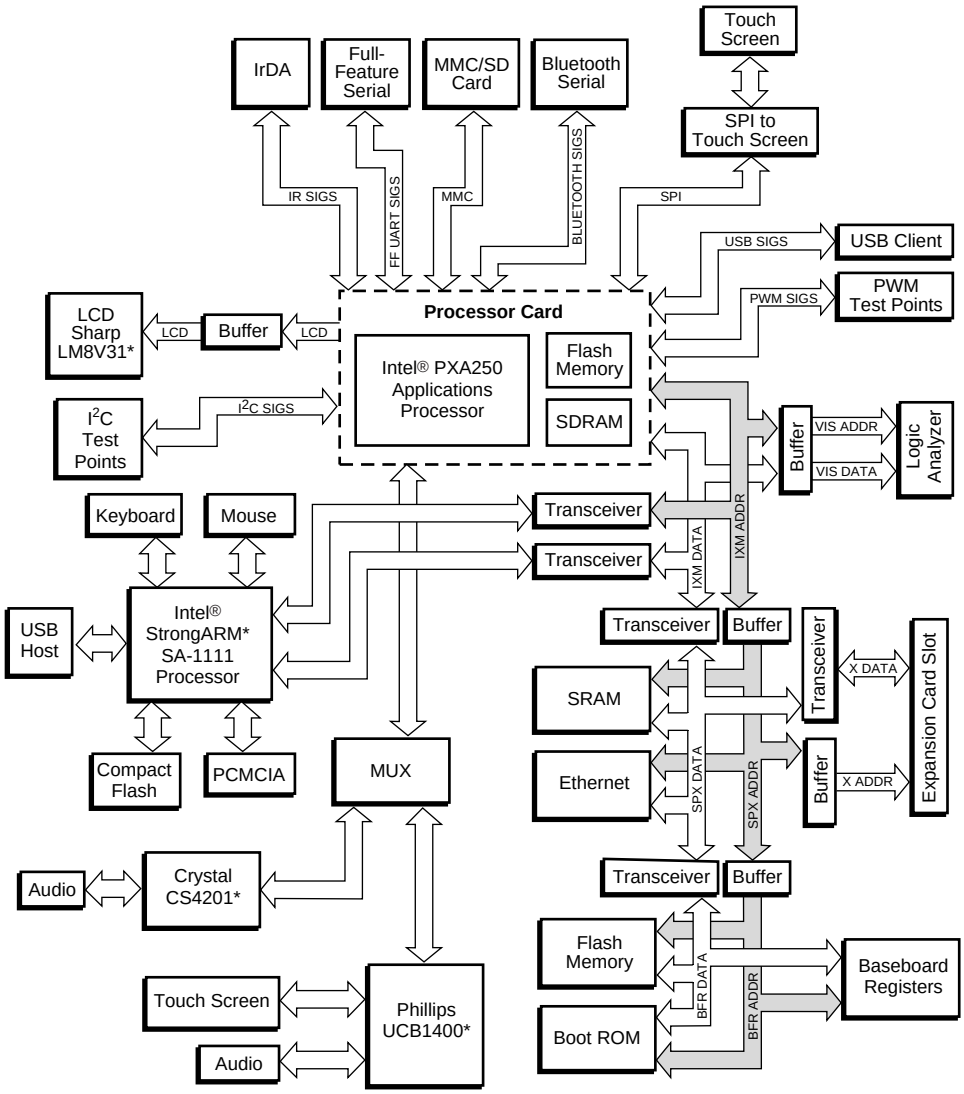
- socketed processor for easy upgrades
- 64 MBytes SDRAM
- two 32-MByte banks of flash memory on the baseboard
- 32 MBytes of flash memory on processor card
- boot from either the baseboard or processor-card flash memory
- 1 MByte SRAM
- one Intel® SA-1111 companion chip, which provides:
  - one PCMCIA slot
  - one Compact Flash slot
  - one USB Host port
  - PS/2 keyboard and mouse support
- Standard Microsystems LAN91C96* Ethernet controller
- touch-screen panel controllers:
  - Philips UCB 1400*
  - Burr Brown ADS7846*
- audio CODECs with microphone, line in, and headphone connectors:
  - Philips UCB 1400
  - Cirrus CS4201*
- Sharp LM8V31 LCD panel, with support for other LCD types
- one USB Client port
- pulse width modulation control
- one infrared (IrDA) transceiver
- full-function and Bluetooth UART serial ports
- one slot for one Secure Digital memory card or MultiMediaCard
- I^2C bus communications
- logic analyzer connections
- one expansion-card slot for custom development
- processor power-supply jumpers for precise power measurements
- eight 7-segment LED digits, eight discrete LEDs, eight discrete switches, and two hexadecimal-encoding switches for use by application software

1.2 System Overview

Figure 1-1 depicts the organization and data flow of the DBPXA250 platform with the DCPXA250 processor card installed.

All communications between the processor and the BBPXA2xx baseboard take place through dedicated or general-purpose PXA250 I/O pins. The general-purpose pins used in the DBPXA250 platform are listed in Section 3.5, “General Purpose Input/Output (GPIO)” on page 3-15. For complete descriptions of these signals, see the *PXA250 and PXA210 Applications Processors Developer’s Manual*.

Figure 1-1. Block Diagram, DBPXA250 Platform



* Other names and brands may be claimed as the property of others.

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1.3 Getting Started

The *Intel® DBPXA250 Development Platform for Intel® Personal Internet Client Architecture Quick Start Guide*, packed in the kit, contains an up-to-date packing list, instructions for setting up and starting the platform, and a discussion of the pass / fail codes displayed by the built-in diagnostics. The quick start guide also contains updates that became available after the publication of this user's guide.

When theDBPXA250 platform has been set up and started without errors, it is ready for use as an applications development system. Detailed operating instructions are found in:

- Chapter 2, "Hardware Description"
- Chapter 3, "Programming Guide"
- The *PXA250 and PXA210 Applications Processors Developer's Manual*

1.4 Related Documents

Effective use of the DBPXA250 platform frequently requires reference to the manufacturer's data sheet for a device. Table 1-1 lists the data items that might be required and the sources for obtaining them.

Table 1-1. Supplemental Documentation (Sheet 1 of 2)

Item	Source
Ault* AC/DC power converter	http://www.aultinc.com
Burr Brown* touch-screen controller	http://www.ti.com
Cirrus* CODEC	http://www.cirrus.com
PXA250 and PXA210 Applications Processors Developer's Manual	http://www.intel.com
PXA250 and PXA210 Application Processors Electrical, Mechanical, and Thermal Specification	http://www.intel.com
Intel® PXA250 and PXA210 Design Guide	http://www.intel.com
Intel® PXA250 and PXA210 Develoment Platforms for Intel® Personal Internet Client Architecture Specification Update	http://www.intel.com
Intel® StrataFlash™ memory	http://www.intel.com
Intel® StrongARM SA-1111 Microprocessor Companion Chip Developer's Manual*	http://www.intel.com
IrDA* infrared transceiver	http://www.agilent.com
Maxim* voltage regulators and control devices	http://www.maximic.com
Philips* UCB 1400 CODEC	http://www.philipssemiconductor.com
Samsung* memory devices	http://www.samsung.com
Sharp* LCD panel	http://www.sharp.com
Standard Microsystems* Ethernet controller	http://www.smsc.com

Table 1-1. Supplemental Documentation (Sheet 2 of 2)

Item	Source
Texas Instruments* voltage regulators	http://www.ti.com
Xilinx* programmable logic devices	http://www.xilinx.com
Intel® DBPXA250 Development Platform for Intel® Personal Internet Client Architecture Quick Start Guide DBPXA250 Development Platform Parts Lists BBPXA2xx Development Baseboard Schematic Diagram DCPXA250 Processor Card Schematic Diagram DCPXA250 and DCPXA210 Specification Update	Intel: Order no. 278403 Order no. 278422 Order no. 278424 Order no. 278425 Order no. 278555

Hardware Description 2

This chapter describes the DBPXA250 platform hardware:

- Section 2.1 — Intel® BBPXA2xx Development Baseboard
- Section 2.2 — Intel® DCPXA250 Processor Card

Using the DBPXA250 platform effectively requires working knowledge of the Intel® PXA250 applications processor (the PXA250 processor). Always refer to the *PXA250 and PXA210 Applications Processors Developer's Manual* for items related to the processor.

The BBPXA2xx baseboard contains several peripheral devices in order to facilitate the development of many different types of applications. The instructions in this chapter and in Chapter 3, "Programming Guide", provide enough details to start operating with minimal effort. In most cases, however, the optimal use of a device — particularly the Intel® StrongARM® SA-1111 Microprocessor Companion Chip — requires detailed reference to the device manufacturer's data sheet. To locate this information, refer to Table 1-1, "Supplemental Documentation" on page 1-4.

Note: The configuration switches on the baseboard and processor card are SPDT slide switches. This document identifies the switch positions as follows:

dot position — the dot on the switch is visible

no-dot position — the dot on the switch is not visible

2.1 Intel® BBPXA2xx Development Baseboard

The BBPXA2xx baseboard accepts the following processor cards:

- DCPXA250 — standard equipment, described in Section 2.2
- DCPXA210 — optional; contact Intel to order the DCPXA210 processor card.

The following sections describe the BBPXA2xx baseboard hardware.

Figure 2-1 shows the baseboard layout and the locations of major components.

Figure 2-2 shows the locations of the switches and jumpers discussed in this section.

Figure 2-1. Component Layout, BBPXA2xx Baseboard

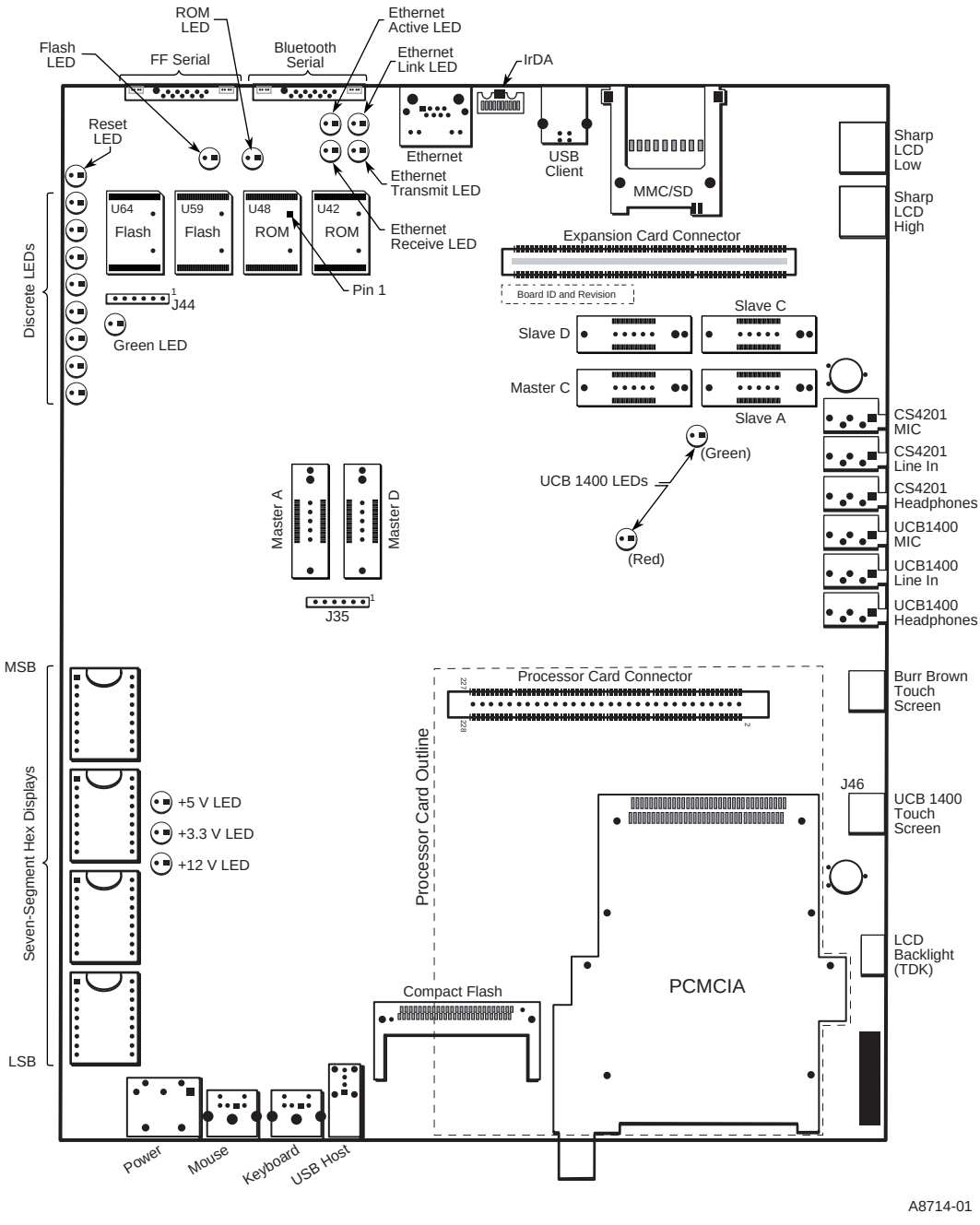
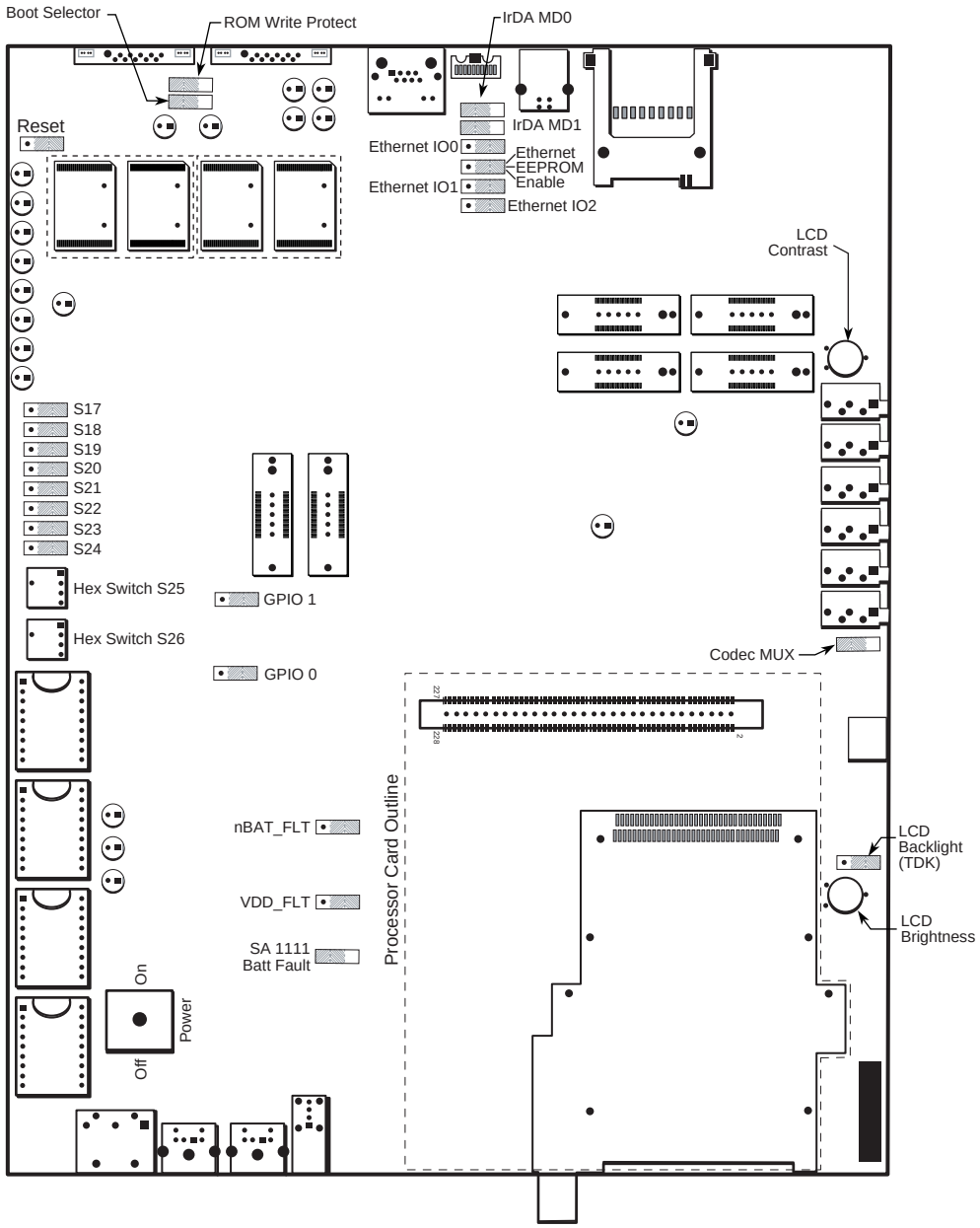


Figure 2-2. Switch, Control, and Jumper Locations, BBPXA2xx Baseboard



2.1.1 Power Supply and Regulation

The DBPXA250 platform derives its power from an external 110 VAC to +12 VDC adapter rated at 6.5 ADC and 75 W. The +12 VDC input is fuse-protected. Switch S16 turns BBPXA2xx baseboard power on and off. Green LED D18 (+12V) indicates power on.

The BBPXA2xx baseboard utilizes a Texas Instruments TPS5102 dual regulator to produce the 3.3 VDC and 5 VDC (VCC) sources from the 12 VDC power input. For more information on this device, refer to the TPS5102 data sheet. Green LEDs D16 (+5V) and D17 (+3.3V) indicate the status of the two voltages.

2.1.2 Fault Switches

Switches S9 (nBAT_FAULT) and S10 (nVDD_FAULT) control the states of the named PXA250 I/O pins. Switch S11 (BAT_FAULT) controls the state of the named SA-1111 pin.

The defaults for these switches is **not asserted**. See Table 2-16 on page 2-20 for the settings.

2.1.3 Reset

Hardware reset switch S27 (RESET) resets both the BBPXA2xx baseboard and the DCPXA250 processor card:

no-dot — assert reset

dot — release reset

Software resets are initiated via the Miscellaneous Write Register (Table 3-7 on page 3-8) by first clearing the appropriate bit to assert the reset, then setting it to release the reset. There are two types of software resets:

Bit PC_RST resets only the processor card.

Bit SYS_RST resets both the processor card and the baseboard.

2.1.4 Flash Memory and Boot ROM

2.1.4.1 Description and Use

The DBPXA250 platform provides three banks of flash memory, each bank of two devices containing 32 MBytes. Table 2-1 summarizes the features of each bank.

Table 2-1. Flash Memory Characteristics

Location	Mounting	Label	Write Protection	Usage Notes
Baseboard	Socketed	ROM	Baseboard switch S14 (nWRPT). **Default** = write-protected (no-dot).	Default boot source (factory code)
Baseboard	Socketed	FLASH	never	Alternate boot source, user applications
Processor Card	Soldered	—	Processor-card switch S3. **Default** = not write-protected (dot)	Alternate boot source, user applications

The three switches listed in Table 2-2 map the PXA250 chip-select signals nCS0 (boot code) and nCS1 among the three flash-memory banks, providing flexibility in usage.

Note: In Table 2-2, the terms **ROM** and **FLASH** indicate the baseboard flash-memory banks. The term **PC** indicates the bank on the processor card. **Bold** print indicates the factory-default settings.

Table 2-2. Flash Memory Usage and Mapping

Baseboard Switch:	Processor Card Switches:		Memory Bank Assigned to Chip Select:	
S15	S1	S2	nCS0†	nCS1
no-dot	**no-dot**	**no-dot**	**ROM**	**FLASH**
no-dot	no-dot	dot	PC	FLASH
no-dot	dot	no-dot	ROM	PC
no-dot	dot	dot	ROM	FLASH
dot	no-dot	no-dot	FLASH	ROM
dot	no-dot	dot	PC	ROM
dot	dot	no-dot	FLASH	PC
dot	dot	dot	FLASH	ROM

† The DBPXA250 platform always boots from the memory bank assigned to nCS0.

For further information on these functions, see the following:

- S1 and S2 — Table 2-21
- S15 — Table 2-16
- Chip selects — Section 3.1, “Memory Map and Chip Selects” on page 3-1.

For information on programming flash memory, refer to Section 3.6, “Programming Flash Memory” on page 3-17.

2.1.4.2 Removing and Installing BBPXA2xx Baseboard Flash-Memory Chips

Caution: Always wear a grounded wrist strap when handling memory chips. When they are removed from the baseboard, store them in an anti-static package. Do *not* touch any part of the chip.

Note: When removing flash memory chips, label them clearly so that they can be replaced in the correct locations.

See Figure 2-1 for the FLASH and ROM chip locations. Orient the platform so that the hex LED displays are at the bottom right.

To remove a flash memory chip, follow these steps:

1. Slide the center lid of the socket down slightly.
2. Open the left-hand socket door by lifting it up and to the left.
   Open the right-hand door by lifting it up and to the right.
3. Using the vacuum pick-up tool, remove the chip from its socket.

To install a flash memory chip, follow these steps:

Caution: Observe the pin-1 orientation as shown in Figure 2-1.

1. Open the socket as described above.
2. Using the vacuum pick-up tool, place the chip flat into its socket.
3. Close first the right-hand socket door, then the left.
4. Latch the socket by sliding the center lid upward until it catches.

2.1.5 Static RAM (SRAM)

Two SRAM devices, organized as 256K by 16 bits, provide 1 MB of general-purpose memory.

SRAM resides in the upper half of the nCS2 chip-select portion of the PXA250 memory map (see Table 3-1 on page 3-1).

2.1.6 PXA250 General-Purpose I/O (GPIO)

Nine of the PXA250 GPIO pins are available to the user on headers J19, J20, and J21 (GPIO). For pin assignments, see Table 2-5 on page 2-14. For details of the GPIO, see Section 3.5, "General Purpose Input/Output (GPIO)" on page 3-15.

GPIO 0 and 1 can be set high or low by switches S13 and S12, respectively. See Table 2-16 on page 2-20.

2.1.7 BBPXA2xx Baseboard Registers and Interrupt Controller

Field-programmable gate arrays implement the BBPXA2xx baseboard registers and the peripheral interrupt controller. These devices can be updated or customized if required — for instructions, see Section 3.7, "Programming Complex Logic Devices" on page 3-19.

Section 3.2, "BBPXA2xx Baseboard Registers" on page 3-2 describes the registers and their programming.

Section 3.4, "Managing Peripheral Interrupts" on page 3-13 describes the interrupt controller and its programming. The following peripherals can generate interrupts on GPIO pin GP0:

- Burr Brown touch-screen controller — Section 2.1.11.2
- Philips UCB 1400 CODEC — Section 2.1.10.1
- Ethernet controller — Section 2.1.17
- PXA250 Client USB — refer to the *PXA250 and PXA210 Applications Processors Developer's Manual*.
- SA-1111 companion chip — Section 2.1.9
- MMC/SD card inserted — Section 2.1.16
- Switch S13 (GP0) — Table 2-16 on page 2-20

A second type of "interrupt" can be generated by switch S12 (GP1), which sets GPIO pin GP1 high or low as shown in Table 2-16 on page 2-20.

2.1.8 LCD Panel and Interface

The BBPXA2xx baseboard has a dedicated connector for the Sharp LM8V31 640x480 STN LCD panel. This display has a built-in touch panel and a CCFT backlight. Manually operated potentiometers on the baseboard provide for contrast and backlight brightness control. Switch S2 provides +5 VDC to a TDK DC-to-AC inverter in the panel, which powers the backlight.

The following display controls are located on the baseboard (see Figure 2-1 for locations):

- R3 (BRIGHT) — LCD brightness
- R1 — LCD contrast
- S2 (TDK) — backlight power on (dot position) or off (no-dot position)

Caution: Do *not* change the setting of S2 while power is applied to the DBPXA250 platform. This might damage the baseboard.

Software can also turn this display on and off with bit LCD_DISP in the Miscellaneous Write Register (see Table 3-7 on page 3-8).

The DBPXA250 platform natively supports only the Sharp display. However, the LCD signals are routed to five sets of 6-pin header connectors. This allows customizing the interface for use with a variety of other LCD panels. For pin assignments, see Section 2.1.20.9, “LCD Connectors” on page 2-15.

2.1.9 Intel® SA-1111™ Microprocessor Companion Chip

The SA-1111 resides in the nCS4 chip-select area of the PXA250 memory map (see Table 3-1 on page 3-1). It provides the interfaces for:

- one PCMCIA slot
- one Compact Flash connector
- one Universal Serial Bus (USB) Host port
- one PS/2 keyboard
- one PS/2 mouse.

The companion chip can generate an interrupt, which can be enabled or masked (Table 3-9 on page 3-10), set or cleared (Table 3-10 on page 3-11). For detailed instructions on programming the SA-1111, refer to the I*ntel® StrongARM® SA-1111 Microprocessor Companion Chip Developer’s Manual*.

2.1.9.1 PCMCIA and Compact Flash

The PCMCIA interface block in the SA-1111 provides control logic and a complete set of signal buffers for one PCMCIA card (J25) and one Compact Flash card (J31), eliminating the need for external control and transceiver components.

The PXA250 PCMCIA and Compact Flash controller communicates with the sockets through dedicated GPIO pins, as shown in Table 3-12, “PXA250 GPIO Map” on page 3-15.

Power to the PCMCIA card is controlled by the SA-1111 GPIO, Bank A. Power to the Compact Flash card is controlled by two bits in the Miscellaneous Write Register, as shown in Table 3-7 on page 3-8.

2.1.9.2 Universal Serial Bus Host Controller

The USB Host controller built into the SA-1111 is compatible with the Open Host Controller Interface, Windows95* USB, and USB Revision 1.1. It supports both low-speed (1.5 Mbps) and high-speed (12 Mbps) USB devices. The USB Host bus is routed to a Type A USB connector, which supplies +5 VDC to the client device.

For details of the external USB interface, see the *Universal Serial Bus Specification Revision 1.1* and the *Open HCI - Open Host Controller Specification for USB*.

2.1.9.3 PS/2 Keyboard and Mouse

These interfaces are designed to communicate with a standard PS/2 trackpad, keyboard, or mouse, using a two-pin serial link. The PS/2 connectors on the BBPXA2xx baseboard are labeled for use with the keyboard or mouse.

2.1.10 Audio CODECs

There are two CODECs on the BBPXA2xx baseboard. Both communicate with the processor through the PXA250 AC97 Controller Unit. Note that the AC97 controller supports only 16-bit audio.

Each CODEC has separate connectors for microphone, line in, line out, and headphones. Each has an integrated headphone amplifier capable of driving headphones or a pair of self-powered speakers. For more information about these CODECs, refer to the manufacturer's data sheet.

Switch S1 (CODEC MUX) selects the CODEC in use:

dot position — Cirrus Crystal CS4201*

no-dot position — Philips UCB1400* (**default**)

Caution: Do *not* change the setting of S1 while power is applied to the DBPXA250 platform. This might damage the baseboard.

In addition to the CODEC, the UCB1400 provides two other functions:

- general-purpose I/O (GPIO) — see Section 2.1.10.1
- the default touch-screen controller — see Section 2.1.11.1

The CODEC MUX switch enables/disables *all three* of the UCB1400 functions. Thus, when the CS4201 CODEC is enabled, the UCB1400 touch-screen controller and GPIO are disabled.

2.1.10.1 Philips UCB1400*

The Philips UCB1400 CODEC supports 20-bit stereo audio with programmable sampling rate, input and output gain control, and digital sound processing.

The UCB 1400 can generate an interrupt, which can be enabled or masked (Table 3-9 on page 3-10), set or cleared (Table 3-10 on page 3-11). Since this device also contains a touch-screen controller, refer to the Philips data sheet for instructions on using the interrupt.

The UCB1400 also has 10 general-purpose I/O (GPIO) pins, described in Table 2-3. Four of these are brought out to J7, a six-pin header. The UCB1400 GPIO is programmed through the PXA250 AC97 interface. For more information on using this GPIO, refer to the Philips data sheet.

Note: The UCB1400 GPIO is disabled when the CODEC_MUX switch is set to deselect the UCB1400.

Table 2-3. UCB1400 GPIO

UCB1400 GPIO	J7 Pin	Function	UCB1400 GPIO	J7 Pin	Function
0	3	Available to user	5	—	Green LED D2
1	4	Available to user	6	—	Red LED D3
2	5	Available to user	7	—	not used
3	6	Available to user	8	—	not used
4	—	not used	9	—	reserved
NOTE: J7 pins 1 and 2 are connected to Ground.					

2.1.10.2 Cirrus Crystal CS4201*

The Crystal CS4201, by Cirrus Logic, is a stereo CODEC designed for PC multimedia systems. This CODEC has a 20-bit digital-to-analog converter and an 18-bit stereo analog-to-digital converter.

2.1.11 Touch-Screen Controllers

The BBPXA2xx baseboard has two touch-screen panel controllers: the Philips UCB1400 and the Burr Brown ADS7846*. Pin assignments for the two connectors are listed in Section 2.1.20.3, “Touch Screen Connector” on page 2-13.

2.1.11.1 UCB1400

The **default** touch-screen controller, contained in the Philips UCB1400 chip on the BBPXA2xx baseboard, communicates with the processor through the PXA250 AC97 controller. Through connector J46, it controls the touch-screen panel built into the Sharp LM8V31 display. This is a four-wire resistive controller supporting position, pressure, and plate resistance measurements.

Note: This touch-screen controller is disabled when the CODEC_MUX switch is set to deselect the UCB1400. Thus, when using the Cirrus CODEC, only the Burr Brown touch-screen controller can be used.

2.1.11.2 Burr Brown ADS7846*

An **alternate** touch-screen controller, the Burr Brown ADS7846, communicates with the processor through the PXA250 Synchronous Serial Port Controller (SSPC), using the Motorola Serial Peripheral Interface* (SPI) protocol. The connector is J5.

When input is pending, the ADS7846 generates an interrupt, which can be enabled or masked (Table 3-9 on page 3-10), set or cleared (Table 3-10 on page 3-11).

To enable the Burr Brown controller, set the TS_nCS bit in the Miscellaneous Write Register (see Table 3-7 on page 3-8). A busy indication is available in the Miscellaneous Read Register (see Table 3-8 on page 3-9).

2.1.12 Pulse Width Modulation

The two PWM signals from the PXA250 processor are connected to test points TP7 (PWM0) and TP5 (PWM1). They are also available on the logic analyzer connectors (see Table 2-10 on page 2-17).

2.1.13 USB Client Port

A Type B USB connector, J30, connects with the PXA250 processor's USB Device Controller interface using dedicated I/O pins.

Insertion and removal of a host or hub device on J30 causes an interrupt, which can be programmed in the Interrupt Mask/Enable Register (Section 3.2.8) and the Interrupt Set/Clear Register (Section 3.2.9). A bit in the Miscellaneous Read Register (Section 3.2.7) can be read to determine whether a USB host or hub device has been inserted or removed.

2.1.14 IrDA Infrared Transceiver

The BBPXA2xx baseboard contains a dual-mode Agilent IrDA transceiver capable of slow infrared (SIR) and fast infrared (FIR) protocols. The IrDA bit in the Miscellaneous Write Register (see Section 3.2.6) controls the transceiver's mode. Switches S3 and S4 control the device's MD0 and MD1 pins, as shown in Table 2-16 on page 2-20. For more information about the transceiver's operation, refer to the Agilent data sheet.

The IrDA transceiver (D5 on the baseboard) communicates with the PXA250 Fast Infrared Communication Port through dedicated GPIO pins IR_RXD and IR_TXD (see Table 3-12, "PXA250 GPIO Map" on page 3-15).

2.1.15 Serial Communications Ports

The PXA250 processor has two UARTs for serial communications: one Full Function (FF) and one Bluetooth (BT). They communicate with the interfaces on the BBPXA2xx baseboard through dedicated GPIO pins, as shown in Table 3-12 on page 3-15. Each connects through a Maxim MAX324CUI RS232 transceiver on the baseboard to a standard DB-9 connector. Pin assignments are the same for both connectors — see Table 2-4 on page 2-14.

Full Function — J43 (FF SERIAL)

Bluetooth — J37 (BT SERIAL)

The PXA250 Bluetooth UART interface is intended to communicate with a Bluetooth baseband controller. It can be used at standard serial levels via the Maxim MAX324CUI RS232 transceiver.

The Bluetooth interface can be modified to operate at CMOS levels. To make this modification, refer to the BBPXA2xx baseboard schematic diagram and follow these steps:

1. Remove the RS232 transceiver chip.
2. Install zero-ohm resistors as shown. This connects the PXA250 Bluetooth lines directly to the RS-232 connector J37.

Caution: Use extreme care when soldering parts. The tiny sizes of the components make soldering very difficult.

2.1.16 MultiMedia / Secure Digital Memory Card

A MultiMediaCard (MMC) or secure digital (SD) memory card can be used in socket J25. It communicates via dedicated I/O pins with the PXA250 MMC controller, using either the MMC or Serial Peripheral Interface (SPI) protocol. For the socket pin assignments, refer to the BBPXA2xx baseboard schematic diagram.

Inserting a card generates an interrupt, which can be enabled or masked (Table 3-9 on page 3-10), set or cleared (Table 3-10 on page 3-11).

The card's "write-protected" status appears in the SD_WP bit in the Miscellaneous Read Register (Table 3-8 on page 3-9).

2.1.17 Ethernet Controller

The Standard Microsystems LAN91C96 Ethernet controller connects to the network through U33, which provides a 10BASE-T (twisted pair) node, supporting IEEE 802.3 operation at 10 Mbps. The controller occupies the nCS3 portion of the PXA250 memory map (see Table 3-1 on page 3-1). For full information on using this controller, refer to the manufacturer's data sheet and to the *PXA250 and PXA210 Applications Processors Developer's Manual*.

The BBPXA2xx baseboard provides the following basic setup, control, and operational features:

- 8- or 16-bit operation, controlled by bit ENET_nEN16 in the Miscellaneous Write register, as shown in Table 3-7 on page 3-8
- Serial EEPROM for configuration. Switch S6 enables and disables the EEPROM (dot = enable).
- 3-bit control lines (IOS) for configuration of the EEPROM's data organization, controlled by switches as follows:

  S5 = IOS0 (dot = 1 for all three switches)
  S7 = IOS1
  S8 = IOS2

- LED indicators as follows:

  D6 (yellow) — Link
  D7 (red) — Transmit
  D8 (yellow) — Board Select
  D9 (yellow) — Receive

- Reset by hardware and software (see Section 2.1.3 on page 2-4).

The LAN91C96 can generate an interrupt, which is enabled or masked (Table 3-9 on page 3-10), set or cleared (Table 3-10 on page 3-11).

2.1.18 Expansion Card Slot

The expansion card slot, J26, occupies the nCS5 portion of the PXA250 memory map (see Table 3-1 on page 3-1). This slot is intended for custom use. Refer to the BBPXA2xx baseboard schematic diagram for the signals available.

2.1.19 User Switches and LEDs

The BBPXA2xx baseboard has eight discrete switches, two hex-encoding rotary switches, eight discrete LEDs, and eight seven-segment hex display digits available for user applications. See the following for instructions on using them:

- Table 2-16, “Switches and Settings, BBPXA2xx Baseboard” on page 2-20
- Table 2-17, “LED Indicators, BBPXA2xx Baseboard” on page 2-21
- Table 3-3, “Hex LED Data Register” on page 3-4
- Table 3-4, “LED Control Register” on page 3-5
- Table 3-6, “User Switches Register” on page 3-7

2.1.20 Connectors and Pin Assignments

For the locations of connectors on the BBPXA2xx baseboard, see Figure 2-1 on page 2-2.

2.1.20.1 Power Input Connector

J45, a DIN-5 connector, accepts +12 VDC power to the BBPXA2xx baseboard. This connector mates with the output of the Ault AC/DC converter provided with the platform:

Pins 3 and 5 — +12 VDC
Pins 1 and 4 — system ground

2.1.20.2 Keyboard and Mouse Connectors

J39 (KYBD) and J42 (MOUSE) are miniature 6-pin DIN connectors wired for standard PS/2 devices. For more information about the interfaces, see Section 2.1.9.3, “PS/2 Keyboard and Mouse” on page 2-8. For pin assignments, refer to the BBPXA2xx baseboard schematic diagram.

2.1.20.3 Touch Screen Connector

J46 provides the connections for the touch-screen panel built into the Sharp display. For more information, see Section 2.1.11.1, “UCB1400” on page 2-9.

Pin 1 — TSPY
Pin 2 — TSMX
Pin 3 — TSMY
Pin 4 — TSPX

J5 (TS BB) provides the connections for an **alternate** touch-screen panel. For more information, see Section 2.1.11.2, “Burr Brown ADS7846*” on page 2-10.

Pin 1 — Y+
Pin 2 — X–
Pin 3 — Y–
Pin 4 — X+

2.1.20.4 Universal Serial Bus Connectors

J36 (USB HOST) is a type A USB connector. For more information, see Section 2.1.9.2, “Universal Serial Bus Host Controller” on page 2-8.

J30 (USB CLIENT) is a type B USB connector. For more information, see Section 2.1.13, “USB Client Port” on page 2-10.

For pin assignments, refer to the schematic diagram.

2.1.20.5 Audio Connectors

The CODECs use standard stereo connectors for audio signals. For more information, see Section 2.1.10, “Audio CODECs” on page 2-8. See the BBPXA2xx baseboard schematic diagram for pin assignments.

J7 — CS4201 MIC
J8— CS4201 LINE IN
J9 —CS4201 LINE OUT
J10 — UCB1400 MIC
J11 — UCB1400 LINE IN
J12 — UCB1400 LINE OUT

2.1.20.6 Serial Communications Port Connectors

Two DB-9 male connectors provide the serial-port interfaces. Pin assignments, shown in Table 2-4, comply with standard RS-232C. For more information, see Section 2.1.15, “Serial Communications Ports” on page 2-10.

J37 (BT SERIAL) serves the PXA250 Bluetooth UART.
J43 (FF SERIAL) serves the PXA250 Full Function UART.

Table 2-4. J37, J43 — Serial Port Connectors

Pin	Signal	Pin	Signal	Pin	Signal
1	DCD	4	DTR	7	RTS
2	RXD	5	Ground	8	CTS
3	TXD	6	DSR	9	RI

2.1.20.7 UCB1400 GPIO Connector

J17 (a six-pin header) provides access to four of the Philips UCB1400 general-purpose I/O pins. For a description and pin assignments, see Section 2.1.10.1, “Philips UCB1400*” on page 2-9.

2.1.20.8 PXA250 GPIO Connector

J19, J20, and J21 (6-pin headers) provide access to the PXA250 GPIO pins listed in Table 2-5. For more information, refer to Section 3.5, “General Purpose Input/Output (GPIO)” on page 3-15.

Table 2-5. J19, J20, J21 (GPIO) — PXA250 GPIO Connectors

J19 Pin	GPIO	J20 Pin	GPIO	J21 Pin	GPIO
1	Ground	1	Ground	1	Ground
2	2	2	5	2	9
3	3	3	nc	3	10
4	4	4	7	4	12
5	nc	5	32	5	nc
6	Ground	6	Ground	6	Ground

2.1.20.9 LCD Connectors

J1 (SHARP LOW), J2 (SHARP HIGH), and J3 (TDK) provide the LCD signals and controls for the Sharp LM8V31 display. See Table 2-6 through Table 2-8 for pin assignments.

J6, J13, J14, J15, and J16 (six-pin headers) supply the LCD signals for custom use with other displays. See Table 2-9 for pin assignments.

For more information, see Section 2.1.8, “LCD Panel and Interface” on page 2-7.

Table 2-6. J1 (SHARP LOW) — LCD Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	16BITL_DD[7]	6	16BITL_DD[2]	11	Ground
2	16BITL_DD[6]	7	16BITL_DD[1]	12	16BITL_LCLK
3	16BITL_DD[5]	8	16BITL_DD[0]	13	B_LCD_DISP
4	16BITL_DD[4]	9	Ground	14	Ground
5	16BITL_DD[3]	10	16BITL_PCLK	15	16BITL_FCLK

Table 2-7. J2 (SHARP HIGH) — LCD Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	Contrast wiper	6	+3.3V	11	16BITL_DD[11]
2	nc	7	16BITL_DD[15]	12	16BITL_DD[10]
3	nc	8	16BITL_DD[14]	13	16BITL_DD[9]
4	Ground	9	16BITL_DD[13]	14	16BITL_DD[8]
5	Ground	10	16BITL_DD[12]		

Table 2-8. J3 (TDK) — LCD Backlight Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	nc	3	Switched +5V backlight power	5	+5V
2	Brightness wiper	4	Ground		

Table 2-9. J6, J13, J14, J15, J16 — Custom LCD Connectors

Pin	Signal	Pin	Signal	Pin	Signal
J6-1	nc	J13-5	16BITL_DD[12]	J15-3	16BITL_DD[6]
J6-2	16BITL_PCLK	J13-6	Ground	J15-4	16BITL_DD[5]
J6-3	nc	J14-1	Ground	J15-5	16BITL_DD[4]
J6-4	16BITL_LCLK	J14-2	16BITL_DD[3]	J15-6	Ground
J6-5	nc	J14-3	16BITL_DD[2]	J16-1	Ground
J6-6	16BITL_FCLK	J14-4	16BITL_DD[1]	J16-2	16BITL_DD[11]
J13-1	Ground	J14-5	16BITL_DD[0]	J16-3	16BITL_DD[10]
J13-2	16BITL_DD[15]	J14-6	Ground	J16-4	16BITL_DD[9]
J13-3	16BITL_DD[14]	J15-1	Ground	J16-5	16BITL_DD[8]
J13-4	16BITL_DD[13]	J15-2	16BITL_DD[7]	J16-6	Ground

2.1.20.10 SD / MMC Socket

J25 is the socket for a MultiMediaCard or secure digital (SD) memory card. For pin assignments, refer to the BBPXA2xx baseboard schematic diagram. For more information on using these cards, see Section 2.1.16, “MultiMedia / Secure Digital Memory Card” on page 2-11.

2.1.20.11 PCMCIA and Compact Flash Sockets

The PCMCIA (J24) and Compact Flash (J31) sockets are described in Section 2.1.9.1 on page 2-7. For pin assignments, refer to the BBPXA2xx baseboard schematic diagram.

2.1.20.12 Processor Card Connector

J29 provides all address, data, control, and GPIO connections between the BBPXA2xx baseboard and the DCPXA250 processor card. For pin assignments, refer to the BBPXA2xx baseboard schematic diagram.

2.1.20.13 Expansion Card Connector

J26 provides the slot for an expansion card, as described in Section 2.1.18 on page 2-12. For pin assignments, refer to the BBPXA2xx baseboard schematic diagram.

2.1.20.14 Reserved Connectors

J18 is reserved for future expansion.

J35 and J44 are used for the programming of complex programmable logic devices (CPLDs) U46 and U53. For more information, refer to Section 3.7, “Programming Complex Logic Devices” on page 3-19.

2.1.20.15 Logic Analyzer Connectors

Six Mictor-38 logic-analyzer connectors provide access to the signals shown in Table 2-10 through Table 2-15. Many of these, particularly the SDRAM signals, are buffered to prevent bus loading.

Table 2-10. J38 (MASTER A) — Logic Analyzer Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	nc	14	ADDR[21]	27	ADDR[7]
2	GND	15	ADDR[20]	28	ADDR[8]
3	nc	16	ADDR[19]	29	ADDR[9]
4	SPARE	17	ADDR[18]	30	ADDR[10]
5	SPARE	18	ADDR[17]	31	ADDR[[11]
6	SDCKLK[2]	19	ADDR[16]	32	ADDR[12]
7	SDCKE[0]	20	ADDR[0]	33	ADDR[13]
8	PWM1	21	ADDR[1]	34	ADDR[14]
9	PWM0	22	ADDR[2]	35	ADDR[15]
10	ADDR[25]	23	ADDR[3]	36	nc
11	ADDR[24]	24	ADDR[4]	37	nc
12	ADDR[23]	25	ADDR[5]	38	nc
13	ADDR[22]	26	ADDR(6]		

Table 2-11. J28 (MASTER C) — Logic Analyzer Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	nc	14	SDRAS	27	RD/WR#
2	GND	15	SDCAS	28	OE#
3	SDCLK[1]	16	SDCLK[0]	29	WE#
4	SDCLK[1]	17	PREG#	30	CS[0]#
5	SDCKE[1]	18	PSKTSEL#	31	CS[1]#
6	SDSC[3]#	19	PWAIT#	32	CS[2]#
7	SDCS[2]#	20	IOIS16#	33	CS[3]#
8	SDCS[1]#	21	PCE[1]	34	CS[4]#
9	SDCS[0]#	22	PCE[2]	35	CS[5]#
10	DQM[3]	23	PIOR#	36	nc
11	DQM[2]	24	PIOW#	37	nc
12	DQM[1]	25	PWE#	38	nc
13	DQM[0]	26	POE#		

Table 2-12. J34 (MASTER D) — Logic Analyzer Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	nc	14	DATA[21]	27	DATA[7]
2	GND	15	DATA[20]	28	DATA[8]
3	nc	16	DATA[19]	29	DATA[9]
4	DATA[31]	17	DATA[18]	30	DATA[10]
5	DATA[30]	18	DATA[17]	31	DATA[11]
6	DATA[29]	19	DATA[16]	32	DATA[12]
7	DATA[28]	20	DATA[0]	33	DATA[13]
8	DATA[27]	21	DATA[1]	34	DATA[14]
9	DATA[26]	22	DATA[2]	35	DATA[15]
10	DATA[25]	23	DATA[3]	36	nc
11	DATA[24]	24	DATA[4]	37	nc
12	DATA[23]	25	DATA[5]	38	nc
13	DATA[22]	26	DATA[6]		

Table 2-13. J23 (SLAVE A) — Logic Analyzer Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	nc	14	USB_INT#	27	L_DD[7]
2	GND	15	SD_CD#	28	L_DD[8]
3	nc	16	RDY	29	L_DD[9]
4	SPX2IXMD#	17	L_FCLK	30	L_DD[10]
5	SPX2IXMD_OE#	18	L_LCLK	31	L_DD[11]
6	BFR2SPXD#	19	L_PCLK	32	L_DD[12]
7	BFR2SPXD_OE#	20	L_DD[0]	33	L_DD[13]
8	X2SPXD#	21	L_DD[1]	34	L_DD[14]
9	X2SPXD_OE	22	L_DD[2]	35	L_DD[15]
10	1111ZIXMD#	23	L_DD[3]	36	nc
11	1111ZIXMD_OE#	24	L_DD[4]	37	nc
12	1111ZIXMA#	25	L_DD[5]	38	nc
13	1111ZIXMA_OE#	26	L_DD[6]		

Table 2-14. J22 (SLAVE C) — Logic Analyzer Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	nc	14	BITCLK	27	GP5
2	GND	15	SSP_RXD	28	GP7
3	nc	16	SSP_TXD	29	GP9
4	FF_RXD	17	SSP_SFRM	30	GP10
5	FF_TXD	18	SSP_SCLK	31	GP11_VIS
6	BT_RXD	19	TS_nCS	32	GP12
7	BT_TXD	20	GPIO_INT#	33	GP13
8	IR_RXD	21	GPIO_SWT0	34	GP14
9	IR_TXD	22	GP0	35	SSP_EXTCLK
10	nAC_RST	23	GP1	36	nc
11	AC_SYNC	24	GP2	37	nc
12	AC_SOUT	25	GP3	38	nc
13	AC_SDIN	26	GP4		

Table 2-15. J27 (SLAVE D) — Logic Analyzer Connector

Pin	Signal	Pin	Signal	Pin	Signal
1	nc	14	PWR_EN	27	SDA
2	GND	15	SP2_RST#	28	SCL
3	nc	16	SDB_RST#	29	MMCCSO
4	ROMCS#	17	POC_RST#	30	MMDAT
5	FLASH_CS#	18	nBATT_FAULT	31	MMCMD
6	SRAM_CS2H#	19	nVDD_FAULT	32	MMCLK
7	REG_CS2H#	20	S1_PWR1	33	SMSC_INT#
8	ENET_nWE	21	S1_PWR0	34	1400_IRQ
9	ENET_nOE	22	S0_PWR3	35	11111_INT
10	ENET_nIORD	23	S0_PWR2	36	MMCLK
11	ENET_nIOWR	24	S0_PWR1	37	nc
12	nRESET	25	S0_PWR0	38	nc
13	nRESET_OUT	26	18V_CE#		

2.1.21 Switches

Table 2-16 describes the functions and settings of the switches on the BBPXA2xx baseboard. See Figure 2-2 for the switch locations. **Boldface print** indicates factory default settings.

Caution: Do *not* change the setting of S1 or S2 while power is on.

Table 2-16. Switches and Settings, BBPXA2xx Baseboard (Sheet 1 of 2)

Switch	Name	Function	Reference Section
S1	CODEC MUX	Select the CODEC: dot =CS4201 CODEC selected **no-dot =UCB1400 CODEC selected**	2.1.10
S2	TDK	Sharp LCD backlight on/off: **dot =on** no-dot =off	2.1.8
S3 S4	IrDA MD0 IrDA MD1	IrDA mode-control pins: dot =pin high **no-dot =pin low**	2.1.14
S5 S7 S8	LAN91C96 IOS0 LAN91C96 IOS1 LAN91C96 IOS2	Ethernet controller chip mode-control pins: **dot =open (pin pulled high internally)** no-dot =pin low	2.1.17
S6	LAN91C96 EEPROM	Enable/disable the Ethernet EEPROM: **dot =enabled** no-dot =disabled	2.1.17
S9	nBAT_FLT	State of the PXA250 I/O pin: **dot =not asserted** no-dot =asserted	—
S10	nVDD_FLT	State of the PXA250 I/O pin: **dot =not asserted** no-dot =asserted	—
S11	BAT_FLT (SA-1111)	State of the SA-1111 pin: dot =asserted **no-dot =not asserted**	—
S12 S13	GP1 GP0	Set the states of GPIO pins 0 and 1: **dot =high** no-dot =low	2.1.6
S14	nWRPT	Write-protect ROM boot memory: dot =not write-protected **no-dot =write-protected**	2.1.4
S15	nROMBT	Together with S1 and S2 on the processor card, these three switches determine the nCS<1:0> mapping and thus the usage of the platform's flash memory banks. With S1 and S2 set to route these chip selects to the baseboard, S15 determines the mapping to the FLASH and ROM banks: dot =nCS1 assigned to ROM, nCS0 to FLASH **no-dot =nCS0 assigned to ROM, nCS1 to FLASH** For full mapping details, see Table 2-2. For details of S1 and S2, see Table 2-21.	2.1.4

Table 2-16. Switches and Settings, BBPXA2xx Baseboard (Sheet 2 of 2)

Switch	Name	Function	Reference Section
S16	Power switch	ON / OFF	2.1.1
S17 S18 S19 S20 S21 S22 S23 S24	DISSW[15] DISSW[14] DISSW[13] DISSW[12] DISSW[11] DISSW[10] DISSW[9] DISSW[8]	User switches: **dot =high** no-dot =low	2.1.19
S25 S26	Hex encoder [7:4] Hex encoder [3:0]	0x0 – 0xF (**0x0**) 0x0 – 0xF (**0x1**)	2.1.19
S27	RESET	System reset, both baseboard and processor card: **dot =reset released** no-dot =reset asserted	2.1.3

2.1.22 Jumpers

Caution: Jumper header J40 is reserved. The jumper must be installed.

2.1.23 LED Indicators

Table 2-17 describes the functions of the LED indicators on the BBPXA2xx baseboard. See Figure 2-1 on page 2-2 for their locations.

Table 2-17. LED Indicators, BBPXA2xx Baseboard (Sheet 1 of 2)

Reference Designator	Function	Notes	Color
U73†	HEX DIGITS 1 & 2	User read/writable	Green
U72†	HEX DIGITS 3 & 4	User read/writable	Green
U71†	HEX DIGITS 5 & 6	User read/writable	Green
U70†	HEX DIGITS 7 & 8	User read/writable	Green
D2	CODEC_GRN_LED	User writable	Green
D3	CODEC_RED_LED	User writable	Red
D6	nLNKLED	Ethernet Link LED	Green
D7	nTXLED	Ethernet Transmit LED	Red
D8	nBSELED	Ethernet Board Select LED	Yellow
D9	nRXLED	Ethernet Receive LED	Yellow
D12	ROM	ROM enabled as boot ROM	Green
D15	FLASH	FLASH bank enabled as boot ROM	Green
D16	VCC (5V)	Voltage present on 5V rail	Green
D17	3.3V	Voltage present on 3.3V rail	Green

Table 2-17. LED Indicators, BBPXA2xx Baseboard (Sheet 2 of 2)

Reference Designator	Function	Notes	Color
D18	ON	Voltage present on 12V rail	Green
D19	GRN_LED	User read/writable	Green
D20	nRESET	Reset LED (RED)	Red
D21	LED[7]	User read/writable	Green
D22	LED[6]	User read/writable	Green
D23	LED[5]	User read/writable	Green
D24	LED[4]	User read/writable	Green
D25	LED[3]	User read/writable	Green
D26	LED[2]	User read/writable	Green
D27	LED[1]	User read/writable	Green
D28	LED[0]	User read/writable	Green
† Hex display decimal points are not connected.			

2.1.24 Test Points

Table 2-18 lists the test points on the BBPXA2xx baseboard.

Table 2-18. Test Points, BBPXA2xx Baseboard

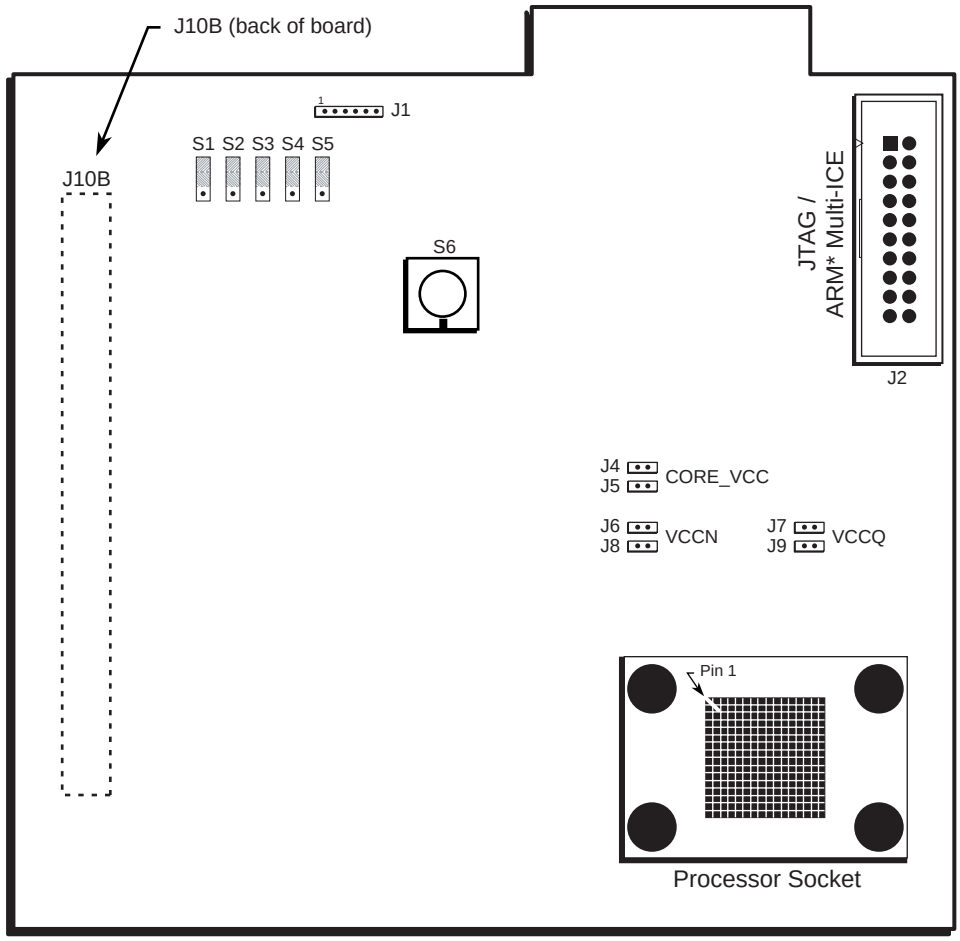
TP	Color	Description	TP	Color	Description	TP	Color	Description
1	Red	LCD_VEE	19	Red	CFV+	37	Red	reserved
2	Ylw	B_LCD_DISP	20	Ylw	IRDA_MODE	38	Red	reserved
3	Ylw	reserved	21	Blk	Ground	39	Red	+12V
4	Ylw	SSP_EXTCLK	22	Red	PWR_USB	40	Blk	Ground
5	Ylw	PWM1	23	Ylw	USB_PLUS	41	Blk	Ground
6	Ylw	L_BIAS	24	Ylw	USB_MINUS	42	Blk	Ground
7	Ylw	PWM0	25	Red	VCC	43	Ylw	SP2_CLK
8	Red	VIN_INV	26	Red	reserved	44	Red	+3.3V
9	Red	+5VA	27	Ylw	TPCLK	45	Red	+3.3V
10	Ylw	SCL	28	Red	reserved	46	Red	VCC
11	Ylw	PWR_EN	29	Red	reserved	47	Ylw	18V_CE#
12	Ylw	X_SDCLK[2]	30	Red	+2.5V	48	Blk	GND
13	Ylw	SDA	31	Blk	Ground	49	Ylw	Reset state
14	Ylw	UDC–	32	Red	reserved	50	Ylw	Reset switch state
15	Ylw	UDC+	33	Ylw	TPDATA	51	Red	VCC
16	Ylw	PWM0	34	Blk	Ground	52	Red	+3.3V
17	Ylw	PWM1	35	Red	+12V	53	Red	VCC
18	Red	PCMCIAV+	36	Red	reserved			

2.2 Intel® DCPXA250 Processor Card

Note: This revision of the *Intel® DBPXA250 Development Platform for Intel® Personal Internet Client Architecture User's Guide* pertains to Revisions E and F of the DCPXA250 processor card.

The DCPXA250 processor card contains the PXA250 processor, SDRAM, and the voltage regulators for the processor. It plugs into J29 on the BBPXA2xx baseboard. Figure 2-3 shows the card's layout.

Figure 2-3. Component Layout, DCPXA250 Processor Card



2.2.1 Removing and Installing the DCPXA250 Processor Card

Caution: Always wear a grounded wrist strap when handling the processor card. When it is removed from the DBPXA250 platform, store it in an anti-static package. Do *not* touch any part of the card except the edges.

To remove the processor card from the baseboard, follow these steps:

1. Orient the platform as shown in Figure 2-3.
2. Grasp the board at the left-hand and right-hand edges. While gently working the right-hand edge up and down, apply upward pressure on the left-hand edge until the card is free.

To install the processor card, follow these steps:

1. Orient the platform as shown in Figure 2-3.
2. Align the large connector on the bottom of the card with its receptacle on the I/O baseboard.
3. Let the processor card slip into its receptacle. When correctly positioned, it will not be free to move in the horizontal plane.
4. Grasp the board at the left-hand and right-hand edges. While gently working the right-hand edge up and down, apply downward pressure on the left-hand edge until the card is firmly seated in its receptacle.

2.2.2 PXA250 Applications Processor

The PXA250 processor is a “system on a chip” based on the Intel® XScale™ microarchitecture. It is specifically designed for applications that require high performance, small size, and low power. The processor’s I/O implementations are described in Section 2.1, “Intel® BBPXA2xx Development Baseboard” on page 2-1.

2.2.3 Removing and Installing the PXA250 Processor Chip

The PXA250 processor is socketed to allow quick replacement. The only tool required is the vacuum-bulb pick-up tool supplied with the DBPXA250 kit. To remove or install a processor chip, orient the platform as shown in Figure 2-3.

Caution: Always wear a grounded wrist strap when handling the processor chip. When it is removed from the processor card, store it in an anti-static package. Do *not* touch any part of the chip.

To remove the processor chip, follow these steps:

1. Unlatch the processor socket by flipping the latch to the right.
2. Swing the cover to the left to expose the processor chip.
3. Using the pick-up tool, remove the chip from the socket.

To install the processor chip, follow these steps:

1. Unlatch the processor socket by flipping the latch to the right.
2. Swing the cover to the left to expose the contact seat.

3. Using the pick-up tool, drop the chip into the socket. Be sure that it is squarely aligned and lying flat in the socket.

Caution: The gold pin-1 identifier on the chip must be oriented toward the *center* of the processor card, as shown in Figure 2-3.

4. Close the socket cover, applying gentle downward pressure. A “click” sound can be heard when the chip seats correctly.
5. Latch the socket cover by flipping the latch to the left.

2.2.4 Voltage Regulation and Control

Two regulators on the PXA250 processor card obtain their +5 VDC inputs from the BBPXA2xx baseboard and produce the processor’s core voltage (CORE_VCC) and phase-locked loop voltage (PLL_VCC).

2.2.4.1 Core Voltage Regulator

A Maxim* MAX1718EEI regulator produces CORE_VCC. The voltage is controlled by the inputs to the regulator’s data pins. For more information about this regulator, see the Maxim* data sheet.

Data inputs to the CORE_VCC regulator come from either of two sources, selected by switch S4:

- no-dot position (**default**) — the voltage is selected by rotary switch S6. For voltages, see Table 2-19.
- dot position — the regulator’s output is programmed by the PXA250 I^2C bus. For voltages, see Table 2-20.

Note: It is possible to set the regulator’s output to a voltage at which the processor cannot function. If shutdown should occur, move switch S4 to the no-dot position, set switch S6 to 0x2, and reset the system. This procedure restores CORE_VCC to 1.5 VDC.

Table 2-19 shows the CORE_VCC voltage as a function of rotary switch S6 settings.

Table 2-19. Switch-Selected CORE_VCC Voltages

S6 Setting:		Voltage	S6 Setting:		Voltage
Binary	Hex		Binary	Hex	
0000	0	1.60	1000	8	1.20
0001	1	1.55	1001	9	1.15
0010	2	1.50	1010	A	1.10
0011	3	1.45	1011	B	1.05
0100	4	1.40	1100	C	1.00
0101	5	1.35	1101	D	0.950
0110	6	1.30	1110	E	0.900
0111	7	1.25	1111	F	0.850

Table 2-20 shows some representative CORE_VCC voltages as a function of the values received on the I2C bus. To program the I2C serial bus values, refer to the I2C chapter in the *PXA250 and PXA210 Applications Processors Developer's Manual*.

Table 2-20. I2C-Programmable CORE_VCC Voltages

I2C Data	Voltage	I2C Data	Voltage
0b0000_0000	1.60	0b0000_1000	1.20
0b0000_0001	1.55	0b0000_1001	1.15
0b0000_0010	1.50	0b0000_1010	1.10
0b0000_0011	1.45	0b0000_1011	1.05
0b0000_0100	1.40	0b0000_1100	1.00
0b0000_0101	1.35	0b0000_1101	0.95
0b0000_0110	1.30	0b0000_1110	0.90
0b0000_0111	1.25	0b0000_1111	0.85

2.2.5 PXA250 I2C Bus

In addition to controlling the CORE_VCC voltage, the I2C bus may be used for custom purposes, such as interconnecting two DBPXA250 platforms. The I2C signals SCL and SDA appear on test points that can be used for this purpose (see Table 2-18 on page 2-22).

Note: Carefully observe the I2C programming instructions in the *PXA250 and PXA210 Applications Processors Developer's Manual*. Errors can cause swings in CORE_VCC that might shut the platform down. Section 2.2.4.1 describes the use of the I2C bus for CORE_VCC regulation.

2.2.6 SDRAM

Two SDRAM chips, soldered to the DCPXA250 processor card, supply 64 MBytes of SDRAM, organized as 4 Mbits, 16 bits wide, across 4 banks. For more information, refer to the Memory Controller chapter in the *PXA250 and PXA210 Applications Processors Developer's Manual*.

2.2.7 Connectors

Connector J1 is reserved for programming the complex programmable logic device (CPLD) U4. For more information, see **Section 3.7, "Programming Complex Logic Devices" on page 3-19**.

Connector J2 (JTAG/ARM* Multi-ICE*) provides the interface for Joint Test Action Group (JTAG) programming of the DBPXA250 platform flash memory. For programming instructions, see Section 3.6, "Programming Flash Memory" on page 3-17.

Connector J10B provides the interface with the BBPXA2xx baseboard. For pin assignments, refer to the DCPXA250 processor card schematic diagram.

2.2.8 Switches

Table 2-21 and Table 2-22 list the switches on the DCPXA250 processor card and their functions. See Figure 2-3 for the switch locations. **Boldface print** indicates factory default settings.

Table 2-21. Switches and Settings, DCPXA250 Processor Card

Switch	Function
S1 S2	Together with S15 on the baseboard, these three switches determine the nCS<1:0> mapping and thus the usage of the platform's flash memory banks. S1 and S2, by themselves, control the routing of these chip selects between the baseboard and the processor card, as shown in Table 2-22. For full mapping details, see Table 2-2.
S3	Write-protection, processor-card flash memory: **dot =not write-protected** no-dot =write-protected
S4	CORE_VCC voltage selection: dot =programmable via the PXA250 I^2C bus **no-dot =selected by rotary switch S6**
S5	reserved

Table 2-22. Switch-Selectable nCS<1:0> Routing

Switch Settings:		Chip-Select Routing:	
S1	S2	nCS1	nCS0
no-dot	**no-dot**	**baseboard**	**baseboard**
no-dot	dot	baseboard	processor card
dot	no-dot	processor card	baseboard
dot	dot	baseboard	baseboard

2.2.9 Jumpers

Jumper headers provide for precision monitoring of crucial voltage domains on the DCPXA250 processor card. Removing the jumpers allows substituting a precision laboratory power supply in place of the following on-board supplies:

J4, J5 — CORE_VCC

J6, J8 — VCCN

J7, J9 — VCCQ

Note: To reduce inductance in the supply lines, each domain is isolated by a pair of parallel jumpers. They must be removed and replaced as a pair.

Caution: Before attempting this procedure, see the DCPXA250 processor card schematic diagram. Carefully observe all standard laboratory precautions, especially polarity and proper power-on sequence.

2.2.10 Test Points

Table 2-18 lists the test points on the DCPXA250 processor card.

Table 2-23. Test Points, DCPXA250 Processor Card

TP	Color	Description	TP	Color	Description
1	†	reserved	8	Blk	Ground
2	†	reserved	9	Ylw	nRESET
3	†	reserved	10	Ylw	PWR_EN
4	Ylw	SSP_EXTCLK	11	Red	VCCN
5	Red	CORE_VCC	12	Red	VCCQ
6	Red	PLL_VCC	13	Blk	Ground
7	Ylw	3.6864-MHz Oscillator	14	Blk	Ground

† not populated

Programming Guide 3

Note: This revision of the *Intel® DBPXA250 Development Platform for Intel® Personal Internet Client Architecture User's Guide* pertains to Revisions E and F of the DCPXA250 processor card.

The PXA250 processor controls the entire DBPXA250 platform, either by including peripherals in the memory map or by using established PXA250 control modules and I/O lines. In all matters of programming detail, refer to the *PXA250 and PXA210 Applications Processors Developer's Manual*. Other applicable documents are listed in Table 1-1, "Supplemental Documentation" on page 1-4.

This chapter covers the following topics:

- Section 3.1 — Memory Map and Chip Selects
- Section 3.2 — BBPXA2xx Baseboard Registers
- Section 3.3 — PXA250 Memory-Control Registers
- Section 3.4 — Managing Peripheral Interrupts
- Section 3.5 — General Purpose Input/Output (GPIO)
- Section 3.6 — Programming Flash Memory
- Section 3.7 — Programming Complex Logic Devices

3.1 Memory Map and Chip Selects

Table 3-1 details the physical addresses and active-low chip selects (nCSx) for the DBPXA250 platform. For a complete listing of the PXA250 memory map, refer to the Memory Controller section of the *PXA250 and PXA210 Applications Processors Developer's Manual*.

Table 3-1. DBPXA250 Physical Addresses and Chip Selects (Sheet 1 of 2)

Type	A[25]	nCSx	Size	Base Address	Ending Address
Boot flash memory	X	0†	32 MBytes	0x0000_0000	0x01FF_FFFF
Application flash memory	X	1†	32 MBytes	0x0400_0000	0x05FF_FFFF
Baseboard registers	0	2	256 Bytes	0x0800_0000	0x0800_00FF
SRAM	1	2	1 MByte	0x0A00_0000	0x0A0F_FFFF
Ethernet controller	X	3	1 MByte I/O 1 MByte Attribute	0x0C00_0000 0x0E00_0000	0x0C0F_FFFF 0x0E0F_FFFF
Intel® SA-1111 Companion Chip	X	4	4 MBytes	0x1000_0000	0x103F_FFFF

Table 3-1. DBPXA250 Physical Addresses and Chip Selects (Sheet 2 of 2)

Type	A[25]	nCSx	Size	Base Address	Ending Address
Expansion card	X	5	64 MBytes	0x1400_0000	0x17FF_FFFF
SDRAM bank 0	††	††	64 MBytes	0xA000_0000	0xA3FF_FFFF

† nCS0 and nCS1 can be assigned to any of three flash-memory banks on the DBPXA250 platform. The platform always boots from the memory bank assigned to nCS0. For full details, see Section 2.1.4, "Flash Memory and Boot ROM" on page 2-4.

†† SDRAM has dedicated chip selects from the PXA250 SDRAM controller.

3.2 BBPXA2xx Baseboard Registers

The following registers, implemented on the BBPXA2xx baseboard, provide for peripheral configuration and control:

3.2.1 System ID Register

The ID register contains three bit fields that identify the baseboard, the processor card, and the expansion card (if any). See Table 3-2 for descriptions of the fields.

This is a read-only register. Reads from reserved bits should be ignored.

Table 3-2. System ID Register

Physical Address: 0x0800_0000 — System ID Register — Baseboard Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved				Baseboard ID				Expansion Card ID				Processor Card ID			
Reset	1	0	0	0	1	0	0	0	User Defined				see table			

Bits	Name	Description
15:12	-	reserved
11:8	Baseboard ID	Baseboard ID: 1000 = BBPXA2xx
7:4	Expansion Card ID	Expansion Card ID, User Defined: 1111 = hard-wired default Refer to the baseboard schematic diagram. The ID signals from the expansion card, XDC_ID[3:0], are pulled high through resistors on the baseboard. To assign an identify to a custom expansion card, tie XDC_ID[3:0] low on the expansion card to produce the desired hex value.
3:0	Processor Card ID	Processor Card ID: 0000 = DCPXA250 processor card 0001 = DCPXA210 processor card

3.2.2 Hex LED Data Register

This register contains eight read/write bit fields, one for each digit of the seven-segment LED displays on the BBPXA2xx baseboard. To display a hexadecimal digit, write its hex value to the desired bit field. All 32 bits may be written at one time. Table 3-3 describes the bit-field assignments.

It is also possible to blank the digits, as described in Section 3.2.3. For locations and more information about the LEDs, see Figure 2-1 on page 2-2 and Table 2-17 on page 2-21.

Note: 16-bit processors can access only bits [15:0].

Table 3-3. Hex LED Data Register

Physical Address: 0x0800_0010 — Hex LED Data Register — Baseboard Registers

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIGIT8				DIGIT7				DIGIT6				DIGIT5				DIGIT4				DIGIT3				DIGIT2				DIGIT1			
Reset	1	0	0	0	1	0	0	0	1	0	0	0	0	0	1	0	1	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1

Bits	Name	Description
31:28	DIGIT8	U70 = Most Significant Digit: four bits of hex data
27:24	DIGIT7	U70
23:20	DIGIT6	U71
19:16	DIGIT5	U71
15:12	DIGIT4	U72
11:8	DIGIT3	U72
7:4	DIGIT2	U73
3:0	DIGIT1	U73 = Least Significant Digit

3.2.3 LED Control Register

This register contains eight read/write bits to blank the hex LED digits and eight read/write bits to control the eight discrete LEDs. Table 3-4 describes the bit assignments.

For locations and more information about the LEDs, see Figure 2-1 on page 2-2 and Table 2-17 on page 2-21.

Table 3-4. LED Control Register

Physical Address: 0x0800_0040								LED Control Register								Baseboard Registers
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BLANKx								LEDx							
Reset	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1	1

Bits	Name	Description
15:8	BLANKx	Blank the hex LED digits: 0 = digit ON 1 = digit OFF BLANK15 = DIGIT8 (most significant) BLANK14 = DIGIT7 BLANK13 = DIGIT6 BLANK12 = DIGIT5 BLANK11 = DIGIT4 BLANK10 = DIGIT3 BLANK9 = DIGIT2 BLANK8 = DIGIT1 (least significant)
7:0	LEDx	Control the discrete LEDs: 0 = LED ON 1 = LED OFF LED7 = D21 LED6 = D22 LED5 = D23 LED4 = D24 LED3 = D25 LED2 = D26 LED1 = D27 LED0 = D28

3.2.4 Configuration Switches Register

The read-only Configuration Switches Register contains the states of the configuration switches on the BBPXA2xx baseboard.

For locations and more information about the switches, see Figure 2-2 on page 2-3 and Table 2-16 on page 2-20.

Table 3-5. Configuration Switches Register

Physical Address: 0x0800_0050 — Configuration Switches Register — Baseboard Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved														nWRPT	nROMBOOT
Reset	1	0	0	0	1	0	0	0	?	?	?	?	?	?	?	?

Bits	Name	Description
15:2	-	reserved
1	nWRPT	Write-protect the baseboard FLASH memory bank: 0 = FLASH bank is write-protected (switch nWRPT = NO DOT). 1 = FLASH bank is not write-protected (switch nWRPT = DOT).
0	nROMBOOT	Boot from baseboard ROM or FLASH memory bank: 0 = Boot from ROM bank (baseboard switch nROMBT = no-dot). 1 = Boot from FLASH bank (baseboard switch nROMBT = dot). **NOTE:** Depending on processor-card switches S1 and S2, the platform can boot from any of three banks of flash memory. For full details, see Section 2.1.4, "Flash Memory and Boot ROM" on page 2-4.

3.2.5 User Switches Register

The read-only User Switches Register contains the states of the eight discrete user-programmable switches and the two hexadecimal-encoded switches, as shown in Table 3-6.

These switches do not alter the configuration of any DBPXA250 platform hardware and may be used arbitrarily as desired.

For locations and more information about the switches, see Figure 2-2 on page 2-3 and Table 2-16 on page 2-20.

Table 3-6. User Switches Register

Physical Address: 0x0800_0060 — User Switches Register — Baseboard Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DISSWx								S25				S26			
Reset	Reset values assume the states of the switches.															

Bits	Name	Description
15:8	DISSWx	Read the discrete user switches: 0 = NO-DOT position 1 = DOT position DISS15 = S17 DISS14 = S18 DISS13 = S19 DISS12 = S20 DISS11 = S21 DISS10 = S22 DISS9 = S23 DISS8 = S24
7:4	S25	Read the hexadecimal-encoded user switch S25: 4 bits of hex data as set by the user
3:0	S26	Read the hexadecimal-encoded user switch S26: 4 bits of hex data as set by the user

3.2.6 Miscellaneous Write Register

This register can be read or written to provide the software control functions detailed in Table 3-7.

Reserved bits must be written with zeros. Reads from reserved bits should be ignored.

Table 3-7. Miscellaneous Write Register

	Physical Address: 0x0800_0080				Miscellaneous Write Register								Baseboard Registers			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	S1_PWR1	S1_PWR0	reserved	RS232 DTR	TS_nCS	reserved	reserved	LCD_DISP	reserved			IrDA Mode	Green LED	ENET_nEN16	PC RESET	SYS RESET
Reset	0	0	0	1	1	0	0	1	0	0	0	0	0	0	1	1

Bits	Name	Description
15 14	S1_PWR1 S1_PWR0	S1_PWR0 = 0, S1_PWR1 = 1: 3.3V S1_PWR0 = 1, S1_PWR1 = 0: 5V
13	-	reserved
12	RS232 DTR	1 = RS232 Data Terminal Ready: 1 = true
11	TS_nCS	Enable/Disable Burr Brown Touch Screen: 0 = enable 1 = disable
10	-	reserved
9	-	reserved
8	LCD_DISP	Sharp LCD display on/off: 0 = off 1 = on
7:5	-	reserved
4	IrDA Mode	Infrared transceiver mode: 0 = slow (SIR) 1 = fast (FIR)
3	Green LED	Green LED D17: 0 = off 1 = on
2	ENET_nEN16	Ethernet data width: 0 = 16 bits 1 = 8 bits
1	PC_RST	Processor Card Reset: 0 = reset asserted 1 = reset released
0	SYS_RST	System Reset: 0 = reset asserted 1 = reset released

3.2.7 Miscellaneous Read Register

This read-only register may be read to obtain the status of the items listed in Table 3-8. Reads from reserved bits should be ignored.

Table 3-8. Miscellaneous Read Register

Physical Address: 0x0800_0090 — Miscellaneous Read Register — Baseboard Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved						USB CLIENT STATUS	TS_BUSY	ENET_nIOIS16	reserved	RS232_RI	RS232_DSR	RS232_CD	SD_WP	reserved	
Reset	1	0	0	0	1	0	0	?	?	?	?	?	?	?	?	?

Bits	Name	Description
15:10	-	reserved
9	USB CLIENT STATUS	Status of the USB client connector: 0 = connector inserted 1 = connector removed
8	TS_BUSY	Burr Brown Touch Screen Busy: 0 = not busy 1 = busy
7	ENET_nIOIS16	Ethernet data width: 0 = 16 1 = 8
6	-	reserved
5	RS232_RI	RS232 Ring Indicator: 1 = true
4	RS232_DSR	RS232 Data Set Ready: 1 = true
3	RS232_CD	RS232 Carrier Detect: 1 = true
2	SD_WP	MMC / SD Memory card write-protected: 0 = not write-protected 1 = write-protected.
1:0	-	reserved

3.2.8 Interrupt Mask/Enable Register

This read/write register allows masking or enabling the interrupts listed in Table 3-9. For details of the interrupt controller, see Section 3.4, “Managing Peripheral Interrupts” on page 3-13.

To enable an interrupt, set its bit to 1. To mask it, clear its bit to 0. Reserved bits must be written with zeros. Reads from reserved bits should be ignored.

Table 3-9. Interrupt Mask/Enable Register

Physical Address: 0x0800_00C0 — Interrupt Mask/Enable Register — Baseboard Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved									USB CLIENT REMOVE	BB PEN	UCB 1400	ETHERNET	USB CLIENT INSERT	SA 1111	MMC/SD IN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	-	reserved
6	USB CLIENT REMOVE	USB client connector removed
5	BB PEN	Burr Brown touch screen
4	UCB 1400	Philips CODEC
3	ETHERNET	Ethernet controller
2	USB CLIENT INSERT	USB client connector inserted
1	SA 1111	Intel SA-1111 companion chip
0	MMC/SD IN	MMC/SD Memory card insertion

3.2.9 Interrupt Set/Clear Register

This read/write register allows setting or clearing the interrupt bits listed in Table 3-10. For details of the interrupt controller, see Section 3.4, “Managing Peripheral Interrupts” on page 3-13.

To set an interrupt, set its bit to 1. To clear it, clear its bit to 0. Reserved bits must be written with zeros. Reads from reserved bits should be ignored.

Table 3-10. Interrupt Set/Clear Register

Physical Address: 0x0800_00D0 — Interrupt Set/Clear Register — Baseboard Registers

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved									USB CLIENT REMOVE	BB PEN	UCB 1400	ETHERNET	USB CLIENT INSERT	SA 1111	MMC/SD IN
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Name	Description
15:7	-	reserved
6	USB CLIENT REMOVE	USB client connector removed
5	BB PEN	Burr Brown touch screen
4	UCB 1400	Philips CODEC
3	ETHERNET	Ethernet controller
2	USB CLIENT INSERT	USB client connector inserted
1	SA 1111	Intel SA-1111 companion chip
0	MMC/SD IN	MMC/SD Memory card insertion

3.3 PXA250 Memory-Control Registers

Table 3-11 summarizes the PXA250 registers used for memory configuration and control. To use them, refer to the *PXA250 and PXA210 Applications Processors Developer's Manual*, which contains detailed register tables and instructions.

The default value in each register is loaded from boot ROM. To return to the factory configuration, write the defaults to the registers that have been modified.

Table 3-11. PXA250 Memory Control Registers

Symbol	Address	Value	Description
MDCNFG	0x4800_0000	0x0000_1AC9	SDRAM Configuration Register 0
MDREFR	0x4800_0004	0x000B_C018	SDRAM Refresh Control Register
MSC0	0x4800_0008	0x23F2_23F2	Static Memory Control Register 0
MSC1	0x4800_000C	0x3FF4_A441	Static Memory Control Register 1
MSC2	0x4800_0010	0x7FF0_7FF0	Static Memory Control Register 2
MECR	0x4800_0014	0x0000_0000	Expansion Memory (PCMCIA / Compact Flash) Bus configuration register
SXLCR	0x4800_0018	0x0000_0000	LCR value to be written to SDRAM-Timing Synchronous Flash
SXCNFG	0x4800_001C	0x0000_0000†††	Synchronous Static Memory Control Register
SXMRS	0x4800_0024	0x0000_0000	MRS† value to be written to Synchronous Flash or SMROM††
MCMEM0	0x4800_0028	0x0000_0000	Card interface Common Memory Space Socket 0 Timing Configuration
MCMEM1	0x4800_002C	0x0000_0000	Card interface Common Memory Space Socket 1 Timing Configuration
MCATT0	0x4800_0030	0x0000_0000	Card interface Attribute Space Socket 0 Timing Configuration
MCATT1	0x4800_0034	0x0000_0000	Card interface Attribute Space Socket 1 Timing Configuration
MCIO0	0x4800_0038	0x0000_0000	Card interface I/O Space Socket 0 Timing Configuration
MCIO1	0x4800_003C	0x0000_0000	Card interface I/O Space Socket 1 Timing Configuration
MDMRS	0x4800_0040	0x0000_0000	MRS† value to be written to SDRAM
BOOT_DEF	0x4800_0044	0x0000_0000	Read-Only Boot-time register. Contains BOOT_SEL and PKG_SEL values.

† Mode Register Set command value

†† Synchronous Mask ROM is not used in the DBPXA250 platform.

†††This value is for the BBPXA2xx baseboard only. Other systems may require different values.

3.4 Managing Peripheral Interrupts

The BBPXA2xx baseboard interrupt controller, shown in Figure 3-1, provides for programming the interrupts caused by peripheral devices or, in the case of the PXA250 USB client, intended for peripheral devices. These are separate from the PXA250 processor interrupts, which are described in the *PXA250 and PXA210 Applications Processors Developer's Manual*. The interrupts depicted in Figure 3-1 appear on the PXA250 general-purpose I/O (GPIO) pin GP0 as an active-low signal.

When an interrupt occurs, its bit is set to 1 in the Interrupt Set/Clear register (see Table 3-10 on page 3-11). To clear the interrupt, clear its bit to 0.

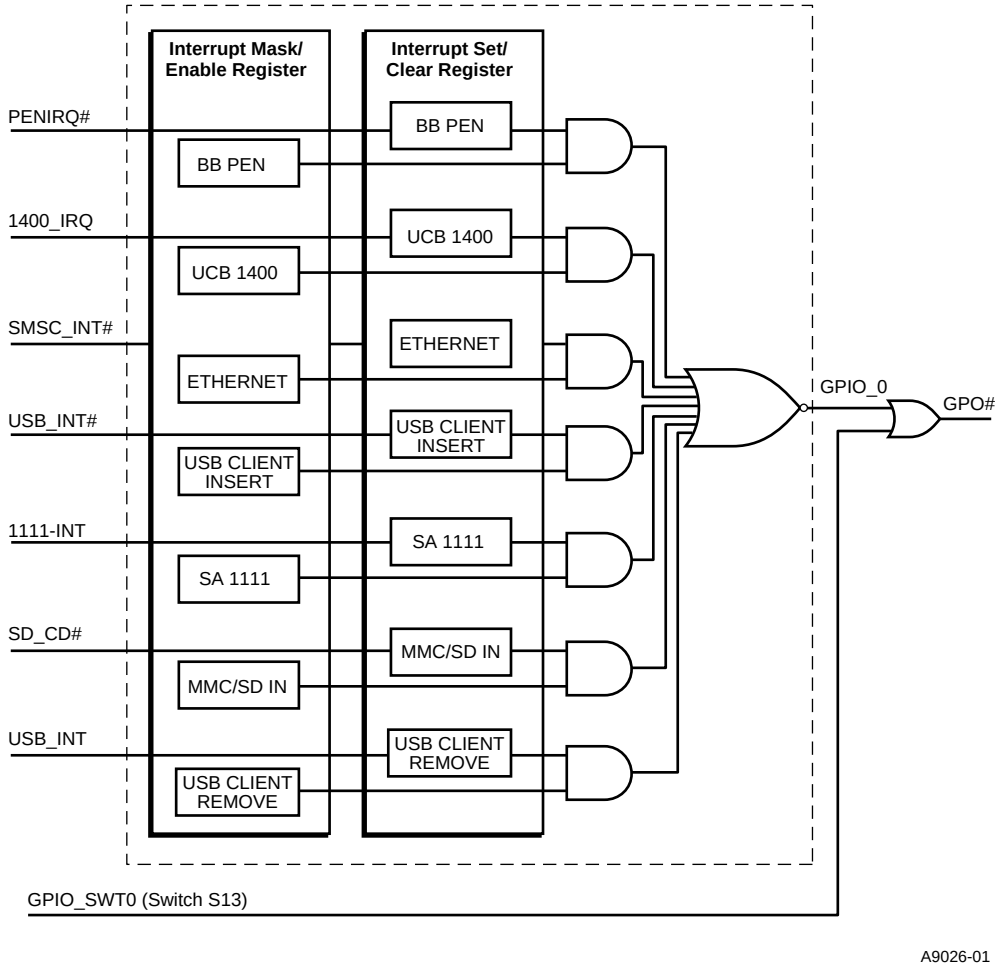
To mask an interrupt, clear its bit to 0 in the Interrupt Mask/Enable Register (see Table 3-9 on page 3-10). To enable it, set its bit to 1.

Switch S13 can also generate an interrupt on pin GP0 (dot position = pin high). This hard-wired signal is not controlled by the interrupt control registers.

A second type of "interrupt" can be generated on pin GP1 by switch S12 (dot position = pin high). This is not shown in the diagram and is not managed by the interrupt control registers.

For more information about these peripherals, refer to the manufacturer's data sheet and to Chapter 2, "Hardware Description".

Figure 3-1. Peripheral Interrupt Controller



3.5 General Purpose Input/Output (GPIO)

The interfaces between the BBPXA2xx baseboard and the DCPXA250 processor card take place through the PXA250 GPIO pins, as shown in Table 3-12.

As shown in the table, nine of these are available for custom use. These are brought out to headers J19, J20, and J21 (GPIO). For pin assignments, see Table 2-5 on page 2-14.

For instructions on programming the GPIO pins, refer to the *PXA250 and PXA210 Applications Processors Developer's Manual*.

Table 3-12. PXA250 GPIO Map (Sheet 1 of 3)

GPIO	Signal Name	GPIO Alternate Function	Direction Relative to Processor	Function
0	GP0	N/A	I	Interrupt generated by U46 (CPLD) Interrupt can also be generated by S13
1	GP1	N/A	I	Interrupt generated by S12
2	GP2	N/A	N/A	Available to user on J19-2
3	GP3	N/A	N/A	Available to user on J19-3
4	GP4	N/A	N/A	Available to user on J19-4
5	GP5	N/A	N/A	Available to user on J20-2
6	MMCLK	AltFn1	O	MultiMedia Card Clock
7	GP7	N/A	N/A	Available to user on J20-4
8	MMCSO	AltFn1	O	MultiMedia Card Chip Select 0
9	GP9	N/A	N/A	Available to user on J21-2
10	GP10	N/A	N/A	Available to user on J21-3
11	GP11	AltFn1	O	3.6864MHz oscillator output
12	GP12	N/A	N/A	Available to user on J21-4
13	MBGNT	AltFn2	O	Memory controller grant
14	MBREQ	AltFn1	I	Memory controller alternate bus master request
15	nCS1	AltFn2	O	Chip Select 1
16	PWM0	AltFn2	O	Pulse width modulation signal, channel 0
17	PWM1	AltFn2	O	Pulse width modulation signal, channel 1
18	RDY	AltFn1	I	Variable latency I/O Device Ready
19	DREQ1	AltFn1	I	DMA request bit 1
20	DREQ0	AltFn1	I	DMA request bit 0
21	GP21	N/A	N/A	Available to user on processor card, U4-143
22	GP22	N/A	N/A	Available to user on processor card, U4-142
23	SSP_SCLK	AltFn2	O	Synchronous Serial Port Clock
24	SSP_SFRM	AltFn2	N/A	Synchronous Serial Port Frame
25	SSP_TXD	AltFn2	O	Synchronous Serial Port Transmit

Table 3-12. PXA250 GPIO Map (Sheet 2 of 3)

GPIO	Signal Name	GPIO Alternate Function	Direction Relative to Processor	Function
26	SSP_RXD	AltFn1	I	Synchronous Serial Port Receive
27	SSP_EXTCLK	AltFn1	N/A	Synchronous Serial Port External Clock
28	AC_BITCLK	AltFn2	O	AC-Link Bit Clock
29	AC_SDIN	AltFn1	I	AC-Link Serial Data In
30	AC_SOUT	AltFn2	O	AC-Link Serial Data Out
31	AC_SYNC	AltFn2	O	AC-Link Sync
32	GP32	N/A	N/A	Available to user on J20-5
33	nCS5	AltFn2	O	Chip Select 5
34	FF_RXD	AltFn1	I	Full Function UART Receive Data
35	FF_CTS	AltFn1	I	Full Function UART Clear to Send
36	FF_DCD	AltFn1	I	Full Function UART Data Carrier Detect
37	FF_DSR	AltFn1	I	Full Function UART Data Set Ready
38	FF_RI	AltFn1	I	Full Function UART Ring Indicator
39	FF_TXD	AltFn2	O	Full Function UART Transmit Data
40	FF_DTR	AltFn2	O	Full Function UART Data Terminal Ready
41	FF_RTS	AltFn2	O	Full Function UART Request to Send
42	BT_RXD	AltFn1	I	Bluetooth UART Receive
43	BT_TXD	AltFn2	O	Bluetooth UART Transmit
44	BT_CTS	AltFn1	I	Bluetooth UART Clear to Send
45	BT_RTS	AltFn2	O	Bluetooth UART Request to Send
46	IR_RXD	AltFn2	I	IrDA UART Receive Data
47	IR_TXD	AltFn1	O	IrDA UART Transmit Data
48	nPOE	AltFn2	O	PCMCIA Output Enable
49	nPWE	AltFn2	O	PCMCIA Write Enable
50	nPIOR	AltFn2	O	PCMCIA I/O Read
51	nPIOW	AltFn2	O	PCMCIA I/O Write
52	nPCE1	AltFn2	O	PCMCIA Card Enable low byte lane
53	nPCE2	AltFn2	O	PCMCIA Card Enable high byte lane
54	nPSKTSEL	AltFn2	O	PCMCIA Socket Select
55	nPREG	AltFn2	O	PCMCIA Register Select
56	nPWAIT	AltFn1	I	PCMCIA Wait
57	nPIOIS16	AltFn1	I	PCMCIA I/O is 16 bits wide
58	L_DD0	AltFn2	O	LCD data pin 0
59	L_DD1	AltFn2	O	LCD data pin 1
60	L_DD2	AltFn2	O	LCD data pin 2
61	L_DD3	AltFn2	O	LCD data pin 3

Table 3-12. PXA250 GPIO Map (Sheet 3 of 3)

GPIO	Signal Name	GPIO Alternate Function	Direction Relative to Processor	Function
62	L_DD4	AltFn2	O	LCD data pin 4
63	L_DD5	AltFn2	O	LCD data pin 5
64	L_DD6	AltFn2	O	LCD data pin 6
65	L_DD7	AltFn2	O	LCD data pin 7
66	L_DD8	AltFn2	O	LCD data pin 8
67	L_DD9	AltFn2	O	LCD data pin 9
68	L_DD10	AltFn2	O	LCD data pin 10
69	L_DD11	AltFn2	O	LCD data pin 11
70	L_DD12	AltFn2	O	LCD data pin 12
71	L_DD13	AltFn2	O	LCD data pin 13
72	L_DD14	AltFn2	O	LCD data pin 14
73	L_DD15	AltFn2	O	LCD data pin 15
74	L_FCLK	AltFn2	O	LCD Frame Clock
75	L_LCLK	AltFn2	O	LCD Line Clock
76	L_PCLK	AltFn2	O	LCD Pixel Clock
77	L_BIAS	AltFn2	O	LCD AC Bias Drive
78	nCS2	AltFn2	O	Chip Select 2
79	nCS3	AltFn2	O	Chip Select 3
80	nCS4	AltFn2	O	Chip Select 4

3.6 Programming Flash Memory

This section describes how to program flash memory to update its code or adapt it for custom use. Flash-memory programming requires the JFlash* programming software and additional files, the Memec Insight* JTAG cable (the JTAG cable) supplied with the DBPXA250 platform, and a host computer system.

To program a flash memory bank on the BBPXA2xx baseboard or the DCPXA250 processor card, follow the instructions set out in the following subsections:

1. Section 3.6.1 — Obtaining the JFlash* Software
2. Section 3.6.2 — Hardware Setup
3. Section 3.6.3 — Programming Instructions

3.6.1 Obtaining the JFlash* Software

To obtain the JFlash* software and additional files, contact the appropriate Intel field sales representative, or visit Intel's web site at:

http://www.intel.com/design/pca/applicationsprocessors/schems/index.htm.

To install the JFlash application on the host computer system, refer to the JFlash software documentation.

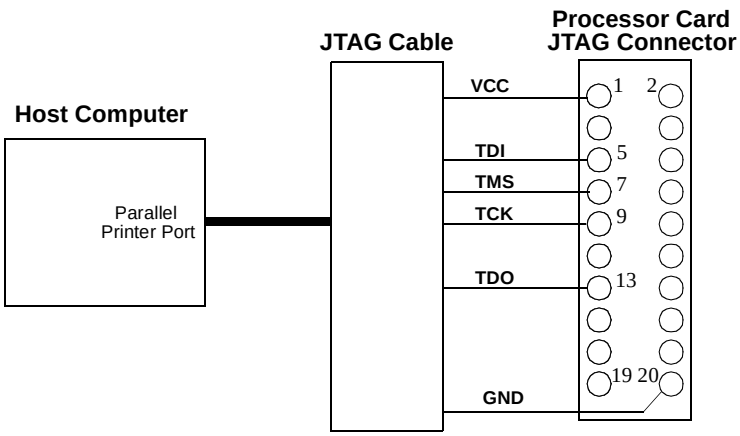
3.6.2 Hardware Setup

Caution: Before setting up the hardware for programming, remove power from the DBPXA250 platform.

1. The programming target (the flash memory bank to be programmed) is always the bank selected by chip-select nCS0, as detailed in Table 2-2, "Flash Memory Usage and Mapping" on page 2-5. Set baseboard switch S15 and processor-card switches S1 and S2 to point to the target bank.
2. When programming the baseboard ROM bank, set baseboard switch S14 to the dot position to remove write-protection.
3. When programming the processor-card bank, set processor-card switch S3 to the dot position to remove write-protection.
4. Connect one end of the JTAG cable to the host computer's parallel port.
5. Connect the other end of the JTAG cable to the JTAG connector on the DCPXA250 processor card, as shown in Figure 3-2.

Caution: Incorrectly attaching the VCC or GND wires will damage the DBPXA250 platform.

Figure 3-2. JTAG Cabling for Flash-Memory Programming



3.6.3 Programming Instructions

1. Obtain the required JFlash files (see section Section 3.6.1).
2. Complete the hardware setup (see Section 3.6.2).
3. Apply power to the DBPXA250 platform.

4. Boot the host computer.
5. Run the JFlash program on the host computer. For operational details, refer to the JFlash software documentation.
6. After programming is complete,
   a. Remove power from the DBPXA250 platform.
   b. Remove the JTAG cable from the JTAG connector on the DCPXA250 processor card.
   c. If necessary, restore the appropriate switch settings if they were modified as described in Section 3.6.2.

3.7 Programming Complex Logic Devices

The DBPXA250 platform has three complex programmable logic devices (CPLDs) that contain control logic for the platform, as described in Table 3-13. This section describes how to reprogram the CPLDs to update their code or adapt them for custom use.

Table 3-13. CPLD Functions and Programming Headers

Device	Function	Header
U53/U54 (FPGA)	Controls the baseboard registers	J44 (baseboard)
U46	Controls data-path directions	J35 (baseboard)
U4	Controls the following: • CORE_VCC voltage selection • Buffer control logic • Other memory-control items	J1 (processor card)

Programming the CPLDs requires the following items:

- A host computer
- Additional files to be installed on the host computer
- Memec Insight* JTAG cable (the JTAG cable), supplied with the DBPXA250 platform kit
- Memec Insight* CD-ROM disk (the Insight CD), supplied with the DBPXA250 platform kit

3.7.1 Obtaining the Required Files

All of the required FPGA and CPLD programming files are compressed into the file *DBPXA250_210_CPLD_source.zip*. To obtain this file, contact the appropriate Intel field sales representative, or visit Intel's web site at:

http://www.intel.com/design/pca/applicationsprocessors/schems/index.htm.

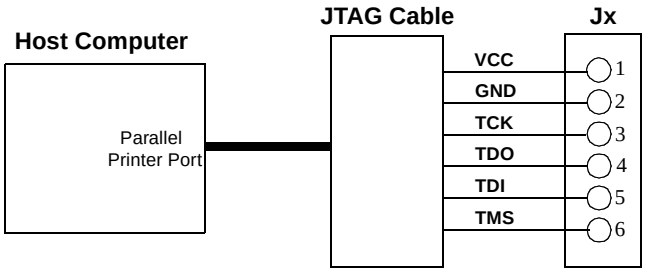
3.7.2 Hardware Setup

Caution: Before setting up the hardware for programming, remove power from the DBPXA250 platform.

1. Slide the DBPXA250 platform reset switch (S27 on the baseboard) to the reset (no-dot) position.
2. Connect one end of the JTAG cable to the host computer's parallel port.
3. Connect the other end of the JTAG cable as shown in Figure 3-2. In this diagram, **Jx** represents the header for programming a specific CPLD, as detailed in Table 3-13.

Caution: Incorrectly attaching the VCC or GND wires will damage the DBPXA250 platform.

Figure 3-3. JTAG Cabling for CPLD Programming



3.7.3 Programming U53/U54

To program U53/U54, complete the following steps:

1. Complete the hardware setup instructions provided in Section 3.7.2.
2. Remove the processor card from the DBPXA250 platform, carefully following the instructions in Section 2.2.1, "Removing and Installing the DCPXA250 Processor Card" on page 2-24.

Caution: Failure to remove the processor card might damage the DBPXA250 platform.

3. From the compressed file obtained as described in Section 3.7.1, extract the files *XC2S100_FG456.bsd* and the most recent version of the file *lubsys*. The *lubsys* file is named using the convention:

   lubsys_X1_X2.mcs, where *X1* is the major revision level and *X2* is the minor revision level.

4. Apply power to the DBPXA250 platform.
5. Boot the host computer.
6. On the host computer, start the Insight CD. Use the instructions on the CD to install Xilinx's device programming software on the host computer.
7. Start the device programming software and use it to program U53/U54.
   a. Use the file *XC2S100_FG456.bsd* when prompted for a BIT or BDSL file for the XC2S100 device.
   b. Use the file *lubsys.mcs* when prompted for an MCS, EXO, or BSDL file for the XC18V01 device.

Note: For instructions on using the device programming software, see the Xilinx web site at www.xilinx.com.

8. After programming is complete,
   a. remove power from the DBPXA250 platform and remove the JTAG cable.
   b. Replace the processor card as described in Section 2.2.1, “Removing and Installing the DCPXA250 Processor Card” on page 2-24.
   c. Restore baseboard switch S27 to its reset-released (dot) position.

3.7.4 Programming U46

To program U46, complete the following steps:

1. Complete the hardware setup instructions provided in Section 3.7.2.
2. Remove the microprocessor from its socket on the DCPXA250 processor card, carefully following the instructions in Section 2.2.3, “Removing and Installing the PXA250 Processor Chip” on page 2-24.

Caution: Failure to remove the microprocessor might damage the DBPXA250 platform.

3. From the compressed file obtained as described in Section 3.7.1, extract the file *JEDEC file lub_bcntl.jed*.
4. Apply power to the DBPXA250 platform.
5. On the host computer, start the Insight CD. Use the instructions on the CD to install the Xilinx XPLA device programming software.
6. Start the device programming software and use it to program U46.

   Use the file *JEDEC file lub_bcntl.jed* when prompted for a design file name for the XCR3128XL device.

Note: For instructions on using the device programming software, see the Xilinx web site at www.xilinx.com.

7. After programming is complete,
   a. remove power from the DBPXA250 platform and remove the JTAG cable.
   b. Replace the microprocessor as described in Section 2.2.3, “Removing and Installing the PXA250 Processor Chip” on page 2-24.
   c. Restore baseboard switch S27 to its reset-released (dot) position.

3.7.5 Programming U4

To program U4, complete the following steps:

1. Complete the hardware setup instructions provided in Section 3.7.2.
2. Remove the microprocessor from its socket on the DCPXA250 processor card, carefully following the instructions in Section 2.2.3, “Removing and Installing the PXA250 Processor Chip” on page 2-24.

Caution: Failure to remove the microprocessor might damage the DBPXA250 platform.

3. From the compressed file obtained as described in Section 3.7.1, extract the file *DCPXA250_U4.jed*.
4. Apply power to the DBPXA250 platform.
5. On the host computer, start the Insight CD. Use the instructions on the CD to install the Xilinx XPLA device programming software.
6. Start the device programming software and use it to program U4.

   Use the file *DCPXA250_U4.jed* when prompted for a design file name for the XCR3128XL device.

Note: For instructions on using the device programming software, see the Xilinx web site at www.xilinx.com.

7. After programming is complete,
   a. remove power from the DBPXA250 platform and remove the JTAG cable.
   b. Replace the microprocessor as described in Section 2.2.3, “Removing and Installing the PXA250 Processor Chip” on page 2-24.
   c. Restore baseboard switch S27 to its reset-released (dot) position.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